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# Electron-Beam Induced Damage in Thin Insulating Films on Compound Semiconductors

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ELECTRON-BEAM INDUCED DAMAGE IN THIN INSULATING FILMS  
ON COMPOUND SEMICONDUCTORS

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Phosphorus rich plasma enhanced chemical vapor deposition (PECVD) of silicon nitride and silicon dioxide films on n-type indium phosphide (InP) substrates were exposed to electron-beam irradiation in the 5 to 40 keV range for the purpose of characterizing the damage induced in the dielectric. The electron-beam exposure was on the range of  $10^{-7}$  to  $10^{-3}$  C/cm<sup>2</sup>. The damage to the devices was characterized by capacitance-voltage (C-V) measurements of the metal insulator semiconductor (MIS) capacitors. These results were compared to results obtained for radiation damage of thermal silicon dioxide on silicon (Si) MOS capacitors with similar exposures.

The radiation induced damage in the PECVD silicon nitride films on InP was successfully annealed out in an hydrogen/nitrogen (H<sub>2</sub>/N<sub>2</sub>) ambient at 400 C for 15 min. The PECVD silicon dioxide films on InP had the least radiation damage, while the thermal silicon dioxide films on Si had the most radiation damage.

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## CHAPTER 1. INTRODUCTION

### 1.1 ELECTRON-BEAM INDUCED DAMAGE

In the past twenty years tremendous progress has been made in the cost, density and performance of silicon (Si) metal-oxide-semiconductor (MOS) integrated circuits. One of the most advanced devices on the market today (1986) is the 1 Mbit DRAM (dynamic random access memory) device with a feature size of 1 micron [1]. This device size will continue to shrink to about half that size before reaching physical limitations.

Electron beam lithography of fine line geometries for microelectronics has become more common as feature sizes continue to shrink. For high frequency devices such as indium phosphide (InP) metal-insulator-semiconductor field effect transistors (MISFETs) and gallium arsenide (GaAs) metal-semiconductor field effect transistors (MESFETs), gate definition by electron beam exposure of photoresist has become a standard practice. However, direct-write electron beam lithography has found only a few application in the production of metal-oxide-semiconductor field effect transistors MOSFETs of very large scale integrated (VLSI) circuits. VLSI technology requires radiation hardness of electronic devices and circuits on both Si and compound semiconductor substrates, because new lithographic techniques use high energy (20-30 keV) electron beams with radiation exposures

on the order of  $10^{-5}$  to  $10^{-4}$  C/cm<sup>2</sup>. These exposures are calculated using a measured beam current, exposed area and time [2,3,4].

## 1.2 ELECTRON-BEAM INDUCED DAMAGE IN OXIDE FILMS ON Si

Electron beam exposure of the sensitive gate insulator and channel region of the Si substrate causes positive charge trapping in the gate and field oxide resulting in large negative threshold voltage ( $V_{th}$ ) shift (as found by capacitance-voltage measurements) and in turn device degradation [2,5,6,7,8].

The existence of these positive trapped charges in the oxide film of the MOS capacitor was verified by Peckerar [9] with temperature bias stressing experiments. In his study, he found that electron-beam and x-ray irradiation of metal (or polysilicon)-oxide-semiconductor (MOS) devices performed at typical photoresist exposure levels created temperature-bias-stress (TBS) instability. His results were explained by assuming that exposure to both of these types of ionizing radiation caused the mobilization of positive charge in the insulator. He applied a large positive gate bias at an elevated temperature to a MOS sample which was previously irradiated at  $10^{-5}$  C/cm<sup>2</sup> with 25 keV electrons. The result was a negative shift in  $V_{th}$ , because the trapped positive charges were forced closer to the semiconductor-gate oxide interface, away from the bias source at the gate ohmic



contact during the bias phase of the TBS test. This damage mechanism was found in hydrochloric (HCl), hydrogen (H<sub>2</sub>)/oxygen (O<sub>2</sub>), and dry grown oxides, where HCl oxides exhibited the least effect of the three oxides.

Peckerar also discovered that nitrogen (N<sub>2</sub>) anneals performed at 500 and 900 C, and H<sub>2</sub> anneals performed at 500 C (all for 30 min) did not substantially reduce TBS instability. But an H<sub>2</sub> anneal performed at 900 C for 30 min did create a marked reduction in the TBS-induced instability.

However, most researchers have discovered that a low temperature anneal at 400 C or less in forming gas (10% H<sub>2</sub> in N<sub>2</sub>) eliminated the positive trapped charge [3,7]. For example, Phillips [2] studied the effect of electron-beam irradiation of typical MOS capacitors with 20 keV electrons. Figure 1.1 shows the functional dependence of the change in V<sub>th</sub> to the electron-beam dosage for isolated and grounded substrates. Phillips also discovered through annealing treatments in flowing N<sub>2</sub> gas of these irradiated samples for five minutes at progressively increasing temperatures, that the change in V<sub>th</sub> decreased gradually with increasing temperatures and approached zero as the temperature approached 400 C (See Figure 1.2).

It was later discovered that normal device operation of these annealed MOS devices resulted in positive shifts in V<sub>th</sub>. These shifts were attributed to the gradual trapping of hot

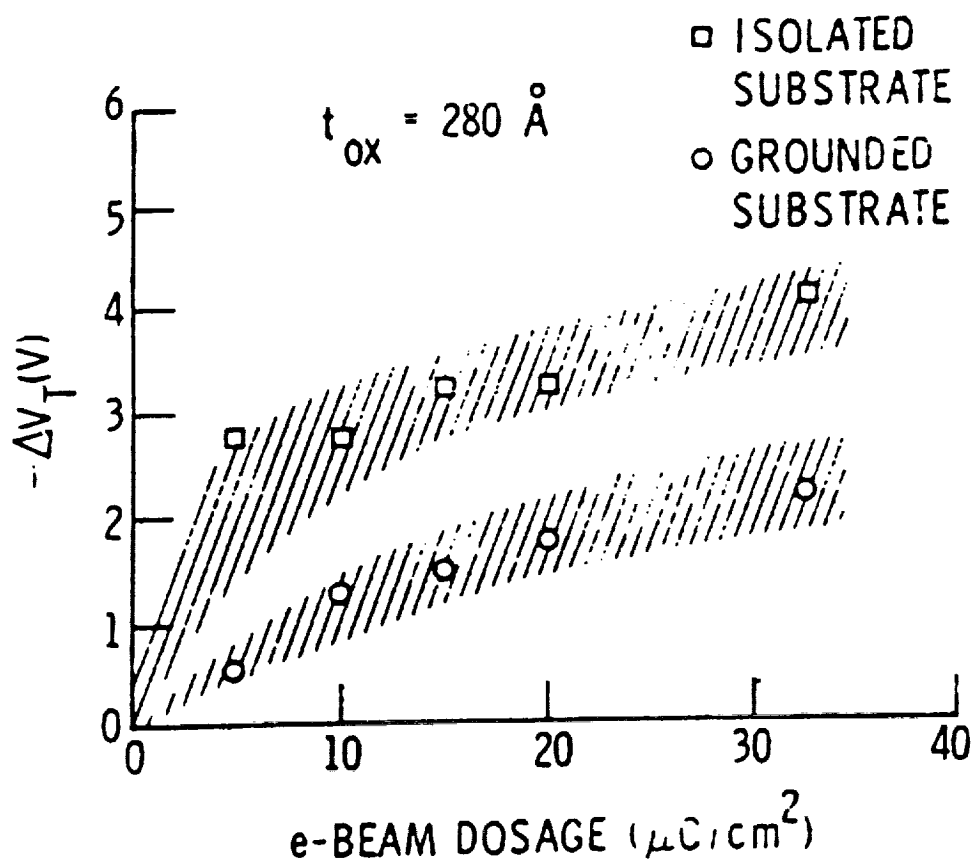


Figure 1.1 shows the functional dependence of the change in  $V_{th}$  to the electron-beam dosage for isolated and ground substrates.

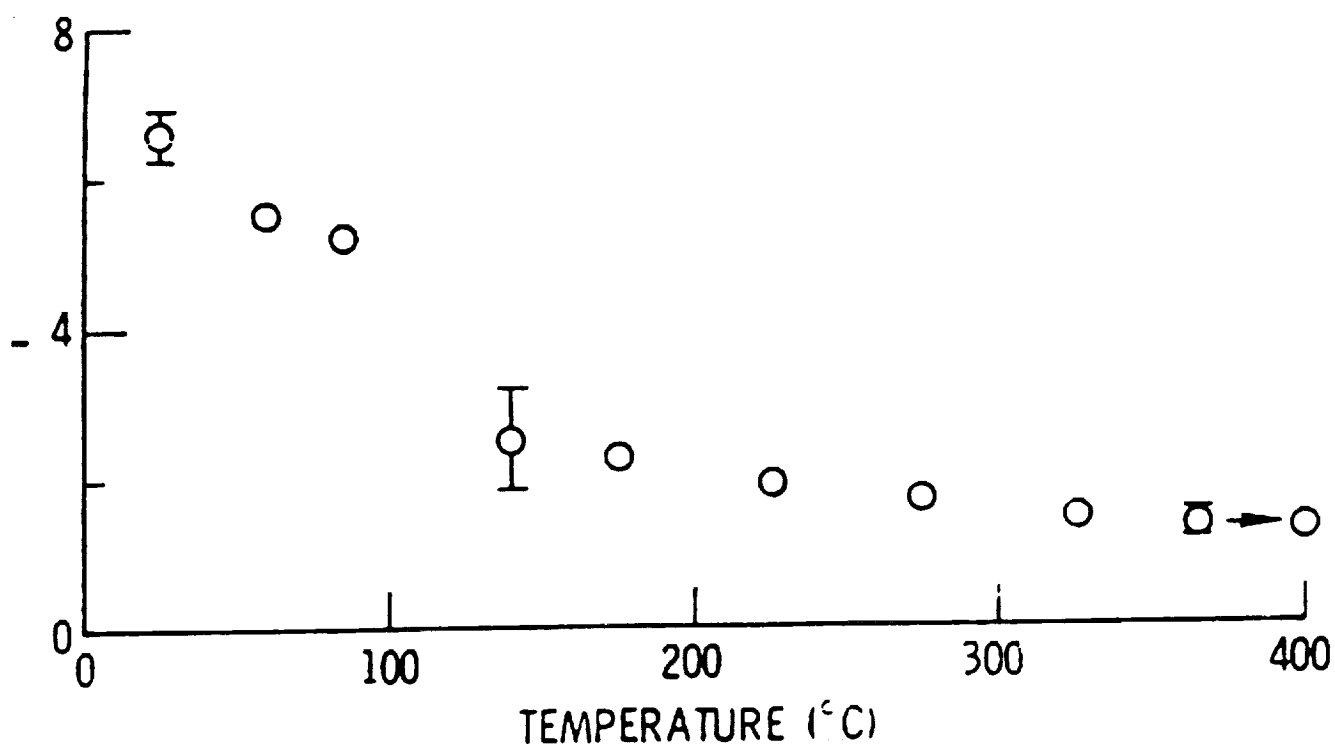


Figure 1.2 shows the change in  $V_{th}$  with increasing temperature.

electrons which were injected into the oxide during device operation. This trapping degraded device performance and eventually lead to an unacceptable low current output [4]. These effects were especially severe for VLSI level devices because of the short channel lengths involved [10].

This electron trapping was due to the presence of neutral traps in the oxide which were caused by electron beam irradiation according to Aitken and Young [3]. They discovered that in addition to the well-known positive space charge, electron-beam irradiated MOS capacitors with 25 keV electrons showed additional uncharged electron traps in the oxide layer. These traps persisted after most of the positively charged defects had been removed by the usual low-temperature ( $\leq 400$  C) anneals. The presence of these neutral traps after the low temperature anneal was determined by the injection of hot electrons into the oxide where they were captured by the existing defects. The effective trap densities increased with increasing electron fluence but were reduced by forming gas anneals at temperatures in excess of 500 C.

These results were later confirmed by Aitken in his study of electron-beam radiation on polysilicon-gate MOSFET's [4]. He irradiated these samples in a vector scan electron-beam lithography system with 25 keV electrons at doses typical of those used to expose electron-beam resists. He showed that in addition to the  $V_{th}$  shift, caused by the accumulation of

radiation-induced positive charge in the gate oxides, these charged centers and additional uncharged (neutral) electron traps lead to an increase in the electron trapping in irradiated oxides. Since these neutral traps were empty, they were not detected by C-V measurements. Only the positive traps showed an effect. In addition, the low temperature anneal did not eliminate the neutral traps but only the positive traps. He also discovered that temperatures above 550 C for 30 min in forming gas were required to anneal both the positive and neutral traps completely from the oxide underlying polysilicon after the exposure to radiation.

Another critical effect of electron beam irradiation on MOS devices that has not been discussed is the increase in the interface state density [6,11,12,13]. Ma, Scoggan and Leone in particular, studied the interface state induced by 25 keV electron beam irradiation in MOS capacitors [14]. For radiation dosage on or above the order of  $1 \times 10^{-5}$  C/cm<sup>2</sup>, all of the radiation-induced interface-state distributions tended to have a similar shape which was asymmetrical about the midgap, independent of the type and concentration of the silicon dopants, and independent of the initial interface-state distributions. The states in the upper half of the silicon band gap were acceptor type which peaked around 0.2 eV from the midgap, whereas the states in the lower half of the band gap were donor type with a lower density.

They found that for radiation dosage below  $1 \times 10^{-7}$  C/cm<sup>2</sup> the postradiation interface states were proportional to their initial values. In addition, from high frequency capacitance-voltage (C-V) measurements they determined that only negatively charged acceptor states between the Fermi level and the midgap contributed to the positive flatband voltage shift in an n-type sample, while only positively charged donor states contributed to the negative flatband voltage shift in p-type samples.

In a MOSFET, interface states will not only cause a  $V_{th}$  shift, but also reduce the transconductance both by trapping electrons in the channel and by reducing their mobility through scattering [15].

In addition, Goetzberger and associates found that interface states have both a DC and an AC effect on MOSFETs [16]. The charge stored in the interface states modifies the electric field at the Si surface, so that more applied voltage is needed to change the surface potential, which results in a stretching out of the C-V curves. This is the DC effect.

The AC effect can be seen as an additional capacitance. Since by definition, an interface state constitutes an additional allowed state at the interface, each interface state adds a capacitance of one elementary charge per state. Therefore this capacitance as a function of surface potential had a sharp peak at the voltage for which the Fermi level crosses the interface

state level. The interface state of charge is determined by its energy relative to the fermi level at the interface, being in a more positive state of charge when it is above the Fermi level. An additional AC effect can be seen by conductance. Since the capture and emission of carriers has a time delay, which can be represented by an RC constant of the interface state, contributes to ohmic losses.

There have been many theories and models to explain the existence of interface states. A few of the more popular are [16]: strained bonds at the interface, charge centers in the oxide, Anderson localization of the charge carrier wave function caused by random potential variation at the interface, structural modification of the silicon dioxide layer, weak bonds at the interface, and trivalent silicon defects at the interface. However it is the last one of these theories that has found some evidence to back it up.

Lenaham and Dressendorfer have studied these trivalent defects [11,17], which are silicon atoms bonded to three other silicon atoms with one unpaired electron. They compared the generation of these radiation-induced  $P_b$  ("trivalent silicon") centers at the silicon/silicon dioxide ( $SiO_2$ ) interface with the radiation-induced buildup of interface states. They observed a strong correlation between the density of  $P_b$  centers and the radiation-induced interface state density ( $D_{it}$ ), including a similar annealing behavior of the radiation-induced  $P_b$  and  $D_{it}$ .

They concluded that  $P_b$  defects accounted for a large portion of radiation induced interface states.

Winokur [18] however feels that the buildup of interface states by ionizing radiation is related to the production of electron-hole pairs in the oxide and the subsequent transport of holes to the Si/SiO<sub>2</sub> interface and not to the direct radiation at the interface or to structural modification of the silicon dioxide layer.

Finally, Wager determined that a low temperature anneal at 350-450 C in a H<sub>2</sub> ambient significantly decreased the interface state density, especially if it was performed after the gate metalization [19].

### 1.3 RADIATION INDUCED DAMAGE IN SILICON NITRIDE FILMS

Silicon nitride also has the qualities of a good insulator such as a wide bandgap, low impurity concentration as well as being stoichiometric, homogeneous and amorphous. In addition, silicon nitride also provides an inert barrier to sodium (Na) and moisture (H<sub>2</sub>O) contamination.

In fact, Sinha and associates studied the properties of amorphous silicon nitride films which had been synthesized from silane (SiH<sub>4</sub>) and ammonia (NH<sub>3</sub>) by reactive plasma deposition at



275 C in an radial flow reactor. They found that plasma enhanced chemical vapor deposition provided an attractive deposition technique for silicon nitride films. Its advantages were: manufacturability, low temperature operation, good step coverage and uniformity, compatibility with Si-gate MOS devices, and great flexibility with regard to control of stresses, film composition, density, and cracking resistance [20].

There have been several studies on the effect of radiation on silicon nitride insulators in metal-nitride-oxide semiconductor (MNOS) devices. It has been known for a number of years that irradiated MNOS devices show a net flatband shift indicating a charging phenomena [21,5,22].

Recently Hughes confirmed this in of irradiated MNOS devices [23]. He concluded that irradiation of silicon nitride films on Si caused photoconductivity due to the production of electron-hole pairs. However, since there is already a large number of both electrons and holes in silicon nitride, this photocurrent was difficult to observe, but could result in charging of the silicon/silicon nitride interface. Therefore he compared experimental data on the charging of MNOS devices under irradiation to solutions of the photoconductivity equations including diffusion, recombination, drift and trapping of the electron-hole pairs (the key ingredient being the diffusion term).

In contrast, Henzel [24] examined silicon nitride dielectric layers and discovered a quite different behavior. Silicon nitride contains a large trap concentration for both electrons and holes, so that no fixed charge was developed in the insulating films after electron beam irradiation.

In another important study of irradiated MNOS devices, Hezel concentrated on the properties of the plasma deposited silicon/silicon nitride interface, namely the fixed nitride charges and the fast interface states [25]. More specifically, he studied the net positive charge density  $Q_N/q$  and the interface state density  $D_{it}$  of MNOS structures on p-type Si (100) with atmospheric pressure chemical vapor deposition (APCVD) and plasma silicon nitride as a function of the nitride deposition temperature and the postdeposition annealing temperature. He found that for APCVD silicon nitride, a decrease in  $Q_N/q$  was accompanied by an increase in  $D_{it}$  with increasing deposition and annealing temperatures.

In addition, he discovered that irradiation with 30 keV electrons at a dosage of  $5 \times 10^{-5}$  C/cm<sup>2</sup> did not affect  $Q_N/q$ , whereas  $D_{it}$  was increased for silicon nitride films deposited below 800 C. For plasma silicon nitride, both  $Q_N/q$  and  $D_{it}$  decreased with deposition and annealing temperatures up to 450 C. He was able to achieve very low interface state densities on the order of  $8 \times 10^9$  cm<sup>-2</sup> eV<sup>-1</sup>. These low  $D_{it}$  values were due to the influence of hydrogen which was incorporated into the PECVD

silicon nitride films. He suggested that large interface state densities could be due to unsaturated bonds at the silicon nitride/silicon interface resulting from incomplete bonding, and could be enhanced by electron bombardment.

#### 1.4 RADIATION DAMAGE IN COMPOUND SEMICONDUCTORS

In the last ten years, considerable interest and effort has been devoted to an increase in the operating speed of electronic devices and the circuits based on them. One possibility for improvement in integrated circuit performance is the use of substrate materials other than silicon. Thus the focus is turned toward compound semiconductors, namely GaAs and InP.

One of the measures of a material to support high speed device operation is the mobility of its electrical charge carriers, especially its electron mobility. Table 1.3 shows that the electron mobilities of GaAs and InP are substantially larger than that of Si, and the same is true of their bandgap. The speed performance of GaAs and InP devices should be further enhanced due to their higher maximum saturated electron drift velocities [26].

In addition, InP has the capability of supporting an oxide based technology because its interface state density is low enough to allow inversion of the surface in a MIS structure,

unlike GaAs. GaAs has such a high interface state density that it pins the fermi level to the lower portion of the bandgap which inhibits accumulation of high mobility electrons at the interface [27]. Therefore, compound semiconductors, especially InP, offer many attractive and potentially advantageous characteristics for high speed, high power, electro-optics and possibly radiation hard circuits [28,29]. However there has not been enough research in the area of radiation effects on deposited insulating films on compound semiconductors to achieve radiation hardness.

Anderson and associates [30] observed the long-term transient responses in enhancement mode InP MISFETs following single 50 ns pulses of 40 MeV electrons at levels between 0.45-10.5 Krads per pulse. The measured change in drain current,  $I_{DS}$ , depended on bias conditions and was between 10-48 % for different devices under high current operating conditions. Recovery times were 50-200 micro-sec and 3ms depending on the device, and all devices exhibited long-term drift in  $I_{DS}$  of longer than 5 min.

When these devices were exposed to gamma radiation while under high current conditions, large  $V_{th}$  shifts were observed at low doses. These shifts were time-dependent, and amounted to a minimum of -0.6 V immediately following a total dose exposure of 5 Krads. The devices were unstable following irradiations and  $V_{th}$  exhibited a drift component for periods longer than 30 min. They concluded that an improvement in the gate insulator must be achieved before these devices could be used for circuit applications in a radiation environment.

TABLE 1.1

SUBSTRATE COMPARISON

Semiconductor	Electron Mobility ( $\text{cm}^2/\text{V-s}$ )	Bandgap (eV)
Silicon	1500	1.12
Gallium Arsenide	8500	1.42
Indium Phosphide	4600	1.35

Table 1.1 Electron mobilities and bandgaps at room temperature for several semiconductors.

In addition, Yamaguchi made a study of minority carrier diffusion lengths and carrier concentrations of room-temperature 1-MeV electron irradiated Zn doped InP substrates. He found that the damage rate for the diffusion length and carrier removal due to irradiation has been strongly decreased with increased carrier concentration of InP. They suggested that this phenomena was caused by the radiation induced defects in the InP interacting with impurity atoms.

## 1.5 THESIS OBJECTIVES

The purpose of this study is to determine the extent of electron-beam induced damage in thin insulating films on a compound semiconductor as a function of exposure time to high energy electron beams.

PECVD silicon nitride and PECVD silicon dioxide films will be deposited on n-type Inp substrates in a capacitively coupled parallel plate reactor using 13.56 MHz RF excitation. Both insulating films will have a very thin phosphorus rich layer at the insulator/semiconductor interface. The silicon nitride films will be deposited using silane ( $\text{SiH}_4$ ), ammonia ( $\text{NH}_3$ ) and nitrogen ( $\text{N}_2$ ) as reactant gases. While the silicon dioxide films will be deposited using  $\text{SiH}_4$  and nitrous oxide ( $\text{N}_2\text{O}$ ) as reactant gases. In addition, a dry thermally grown silicon dioxide sample on p-type silicon was used for comparison.

The thickness and refractive index of the deposited films will be determined by ellipsometry. Then MIS and MOS capacitors will be fabricated in order to evaluate the electrical properties of these films by using current-voltage (I-V) and high frequency (1 MHz) capacitance-voltage (C-V) measurements.

Electron-beam exposures of the MIS and MOS structures will be performed and C-V measurements will be used to determine the extent of damage. In addition, low temperature annealing of the damaged devices will be performed and C-V measurements will again be used to characterize the results.

## CHAPTER 2. EXPERIMENTAL APPARATUS

### 2.1 PLASMA DEPOSITION SYSTEM

All of the insulator depositions were carried out in a Technics Planner Etch PE-IIA plasma system. Operation of this system required a Leybold-Heraeus D16A Trivac vacuum vane pump with an exhaust port and a 1000C Dual Canister oil filtration system consisting of a particulate filter and an aluminum oxide filter was needed. The pump and filter system was filled with a 14/6 grade Fomblin Oil. In addition, a cold water source and drain (no pun intended) and compressed air between 70 to 100 psi was also needed.

The deposition chamber was circular with an area of approximately  $610 \text{ cm}^2$  and a separation between electrodes of 3.0 cm. The chamber and the capacitively coupled parallel plate electrodes were both made of aluminum. The substrates were placed on the grounded lower electrode which could be heated by a resistive coil up to 350 C. The temperature is regulated by a Watlow temperature controller which could be set to  $\pm 1 \text{ C}$ . The chamber pressure was measured using a capacitance manometer and was regulated by an electrically controlled throttle valve in the exhaust line. The chamber pressure was set using a potentiometer on a MKS 262A type exhaust valve controller.[31]



There was one major modification to the deposition system. The built in 30 KHz Rf generator was replaced with a RF Plasma Products model HFS-251s solid state Rf generator which was operated at 13.56 MHz. Using the high frequency, deposition parameters and insulator characteristics were improved [32].

The deposition system also includes a Technics gas controller system which employs three Vacuum General Model 80-4 mass flow controllers. Solenoid valves are electrically controlled using calibrated mass flow sensors with flow rates from 0 to 100 standard cubic centimeters per minute (sccm). The mass flow controllers require calibration factors in order to correct for the flow of different gases. The calibration factors for the gases used in this plasma system are listed in Table 2.1. The reactant gases, namely nitrogen ( $N_2$ ) and nitrous oxide ( $N_2O$ ) in line #1, silane ( $SiH_4$ ) in line #2 and ammonia ( $NH_3$ ) in line #3. All three lines came together into one output valve which ran to an input valve in the back of the deposition system. This input line was controlled by a solenoid valve labeled "Gas 1" on the front of the deposition system (which had to be on in order for the individual mass flow controllers to function. These reactant gases were introduced through a manifold before entering the chamber through the top electrode and flowed radially inward to an exhaust port in the center of the lower electrode. In addition, a Freon-14 ( $CF_4$ ) line (which was used for etching) entered the back of the deposition system through a second input valve and was controlled by a solenoid valve labeled

TABLE 2.1

CALIBRATION FACTORS FOR MASS FLOW CONTROLLERS

<u>Reactant Gases</u>	<u>Calibration Factors</u>
N <sub>2</sub>	1.00
NH <sub>3</sub>	0.68
SiH <sub>4</sub>	0.59
O <sub>2</sub>	1.00
N <sub>2</sub> O	0.73
CF <sub>4</sub>	0.42

Table 2.1. Calibration factors of reactant gases for the mass flow controllers.

"Gas 2" on the front of the system. See Figure 2.1 for the layout of the system.

The gas lines were all stainless steel tubing cleaned with a TCE, Acetone, Methonal degrease. The  $\text{SiH}_4$  line had a Swagelock stainless steel check valve with a viton "O" ring and a Matheson single stage regulator with a back purge. The  $\text{NH}_3$  line had a Swagelock stainless steel check valve with a neoprene "O" ring and a Matheson single stage regulator with a back purge. The  $\text{N}_2$  and  $\text{N}_2\text{O}$  gases shared a common line which was set up the same as the silane line except that the  $\text{N}_2\text{O}$  regulator had a back purge while the  $\text{N}_2$  regulator did not need one purge. Finally, the freon-14 ( $\text{CF}_4$ ) had a Swagelock monel check valve with a viton "O" ring and also a Matheson single stage regulator with a back purge. See Figure 2.2 for a gas flow chart.

Following the initial installation of the entire deposition system, leak testing was performed. In order to evacuate the deposition chamber, the following procedure was followed:

#### INITIAL CHAMBER EVACUATION

- (a) The exhaust fan in the ceiling must be turned on.
- (b) The water must be flowing through the cooling system lines or else the Rf power cannot be turned on.

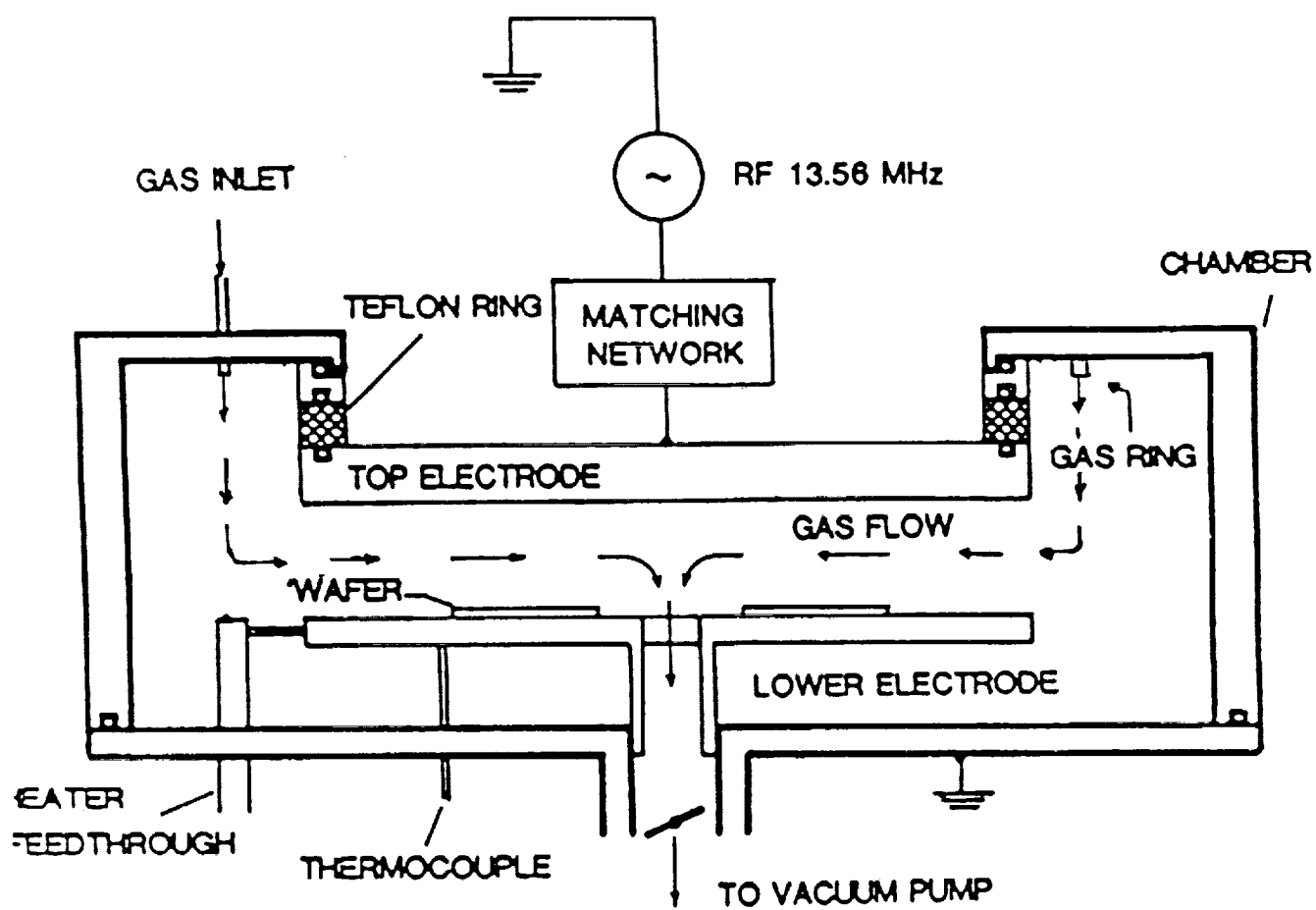


Figure 2.1 Technics Planar Etch PE-IIA direct PECVD deposition system

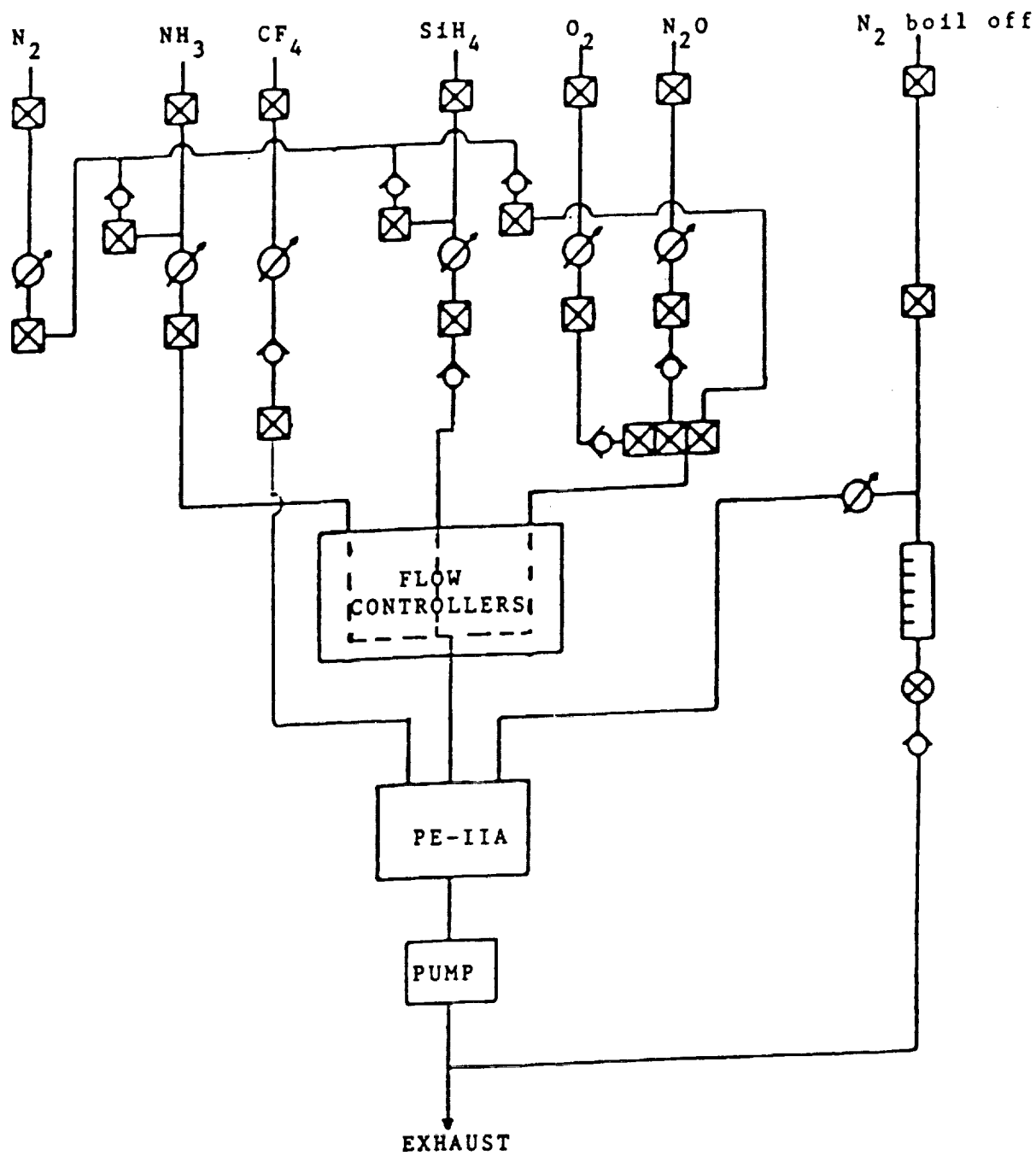


Figure 2.2 Gas flow diagram for the PE-IIA deposition system

- (c) The  $N_2$  vent flow must be on with a pressure of 70 to 100 psi or else the solenoid valve will not open.
- (d) The deposition chamber must be open with the solenoid switch set to open and all of the other valves closed.
- (e) Start the vacuum pump and wait 2 to 5 minutes to let it warm up sufficiently.
- (f) Now close the vacuum chamber tightly and allow the system to evacuate the chamber.

The system was allowed to run for 15 hours and the chamber pressure was only .085 torr. This was not very good, which means there must be a leak in the system somewhere. Therefore, all of the interconnections between the pump and the vacuum chamber had to be taken apart. This included removing all of the KF flanges or clamps and lubricating all of the "O" rings between the connections with vacuum grease or silicone lubricant. In addition, the heat electrode and thermalcouple were removed from the chamber from underneath through the left side panel of the PE IIA. The "O" ring was lubricated inside of these and they were both tightened slightly with a wrench. The last step was to take out and grease the small "O" ring inside the chamber window as well as the large "O" ring around the top cover of the vacuum

chamber. Following the same starting procedure, this time the chamber pumped down to .030 torr in only 15 minutes, and after running for 4 hours the pressure was .016 torr. This means that the chamber is free of leaks, however the gas lines and regulators must now be leak tested.

In order to test the gas lines for leaks, the first step was to get the air out of all of the lines by purging them with nitrogen and then leaving gas pressure in the lines overnight to see if the pressure changes. The following procedure was followed to purge and fill all of the gas lines with N<sub>2</sub>:

#### NITROGEN PURGING

- (i) All of the gas cylinder valves and regulator valves must be closed, as well as all of the mass flow controllers. Follow the procedure on the previous page for evacuating the deposition chamber.
- (ii) Turn the "Gas 1" flow switch on the deposition system to the on position.
- (iii) Switch the N<sub>2</sub> mass flow controller to flow and allow all of the air to be evacuated out of the line, until the chamber pressure reaches below

.100 torr again. Then switch the N<sub>2</sub> flow controller to the off position.

(iv) Open the N<sub>2</sub> cylinder valve (the tank pressure will show up on the regulator, in this case it was 2500 psi.). Then set the desired psi to flow out of the regulator, in this case 100 psi. Finally open the output regulator valve to allow N<sub>2</sub> to flow through all of the N<sub>2</sub> lines. At this point all of the air is out of the N<sub>2</sub> regulator.

(a) Now the N<sub>2</sub> flow controller is switched off and the N<sub>2</sub> output valve on the regulator is turned off as well. Then the flow switch is opened to evacuate the N<sub>2</sub> lines again. This step is repeated three more times in order to get pure N<sub>2</sub> in the lines.

(b) Now the N<sub>2</sub> flow controller is turned off and the N<sub>2</sub> regulator output valve is opened allowing the lines to fill with N<sub>2</sub> once again. Then open the N<sub>2</sub> flow switch and wait until regulated flow occurs before turning off the N<sub>2</sub> flow and closing the N<sub>2</sub> regulator output valve and finally the N<sub>2</sub> cylinder valve. At this point all of the flow valves should be off.



- (v) The silane regulator and lines are next. First of all the silane gas cylinder must be securely closed, as well as all of the regulator valves. Now the gas #2 flow ( $\text{SiH}_4$ ) switch is opened to allow the line to be evacuated to a pressure below .100 torr.
- (vi) The  $\text{N}_2$  cylinder is then opened, followed by the  $\text{N}_2$  regulator output valve.
- (vii) Then the silane regulator output is set at 5 psi.
- (viii) The flow switch for the silane (gas #2) line on the mass flow controller is turned off in order to keep the controller from going out of control when the gas line is opened.
- (ix) Now the  $\text{Si}_3\text{H}_4$  regulator output valve is opened followed by turning the silane flow switch to on and allowing  $\text{N}_2$  to fill the lines.
- (x) Once a constant flow is reached, the silane flow switch is turned off and the silane regulator back purge valve is also turned off leaving the regulator output valve open. This leaves the silane gas line under a pressure of 5 psi.

- (xi) In order to purge the ammonia gas lines, steps five through ten are repeated for gas #3 setting the regulator output pressure at 25 psi.

Leaving the gas lines pressurized overnight showed that there was a leak somewhere in the nitrogen line because the regulator pressure showed zero instead of 100 psi. Using a helium leak detector, a small leak was detected at the "T" joint to the silane body purge in the nitrogen line. The pressure check was repeated after repairing the leak and the system seemed to be leak free.

The final test of the deposition system was to run a nitrogen plasma in the chamber. Steps (a) through (f) on page 5 (this chapter) were followed to evacuate the deposition chamber. Then  $N_2$  gas was allowed to into the chamber at a rate that kept the chamber pressure at .250 torr. The rf power was then turned on and gradually increased until a plasma was ignited. A very clear and purple  $N_2$  plasma appeared at 50 Watts. This meant that the system was now operational and ready for the deposition of the silicon nitride and silicon dioxide films.

## 2.2 ELLIPSOMETRY SYSTEM

The thickness and the refractive index of the PECVD silicon nitride and silicon dioxide, as well as the thermally grown silicon dioxide films were determined using a Gaertner Model L116A Dual Mode Automation Ellipsometry System. The light source was a helium-neon laser that had a wavelength of 6328 Å at an incidence angle of 70 degrees. The thickness and refractive index of the single layer, transparent film was determined by illuminating the sample with monochromatic light of known polarization and analyzing the state of polarization of the reflected light.

Ellipsometry measurements were taken at several different points on each sample in order to determine the uniformity of the films. The measurements were controlled with a Hewlett-Packard Model 85F computer using a BASIC program called "GC5A" supplied by Gaertner. The program needed input parameters of the substrate refractive index, an estimate of the film refractive index, the angle of incidence and the estimated film thickness. The substrate refractive indices for Si and InP, and the film refractive indices for silicon nitride and silicon dioxide that were used are shown in Table 2.2 and 2.3 [33]

TABLE 2.2

SUBSTRATES	INDEX OF REFRACTION	
	Ns	Ks
Si	3.882	-0.020
InP	3.536	-0.307

Table 2.2 shows the refractive indices that were used for the ellipsometry measurements.

TABLE 2.3

INSULATORS	INDEX OF REFRACTION
Silicon Nitride	2.05
Silicon Dioxide	1.46

Table 2.3 shows the refractive indices that the deposition were attempting to obtain.

### 2.3 SCANNING ELECTRON MICROSCOPE

An ISI DS-130 Scanning Electron Microscope was used to irradiate all of the samples. However several modifications were made in order to make C-V measurements without removing the sample from the SEM chamber. This means that electrical connections had to be made to the sample in the chamber prior to irradiation in such a way so that they may be accessed from outside the chamber.

This was accomplished by using a Semi-Conductor Mini-Probe Mount by Ernest F. Fullam Inc. This mount consisted of a 1.5 inch diameter aluminum disc with four probe arm assemblies mounted on the disc. All of the probe arm assemblies were made of brass with stainless steel probes and each arm assembly was floating on the aluminum stage (not grounded to the stage). Each probe arm had a lead wire connected to it. These wire leads were connected to a small 25 pin terminal board located at the lower left side of the specimen chamber door. Each terminal is numbered and connected to a corresponding pin on a terminal outside of the specimen chamber door.

A cable with a 25 pin connector on one end and four coaxial cables with BNC connectors on the other end was constructed to make an electrical connection to the measurement system. The center pins of the four coaxial cables were connected to four pins on the 25 pin connector, namely pins number: 7,9,11 and 23.

The sheath grounds of the four coaxial cables were all connected to pin # 19 as well as to a lead wire coming out of the connector so that it could be separately grounded.

In addition, the SEM chamber was also modified so that two thermalcouple wires could be connected to the sample inside the chamber. This was accomplished by drilling a hole and using a vacuum tight seal in the side of the SEM chamber. The two thermalcouple wires outside of the SEM chamber were connected to a digital thermometer so that the substrate temperature could be monitored during the irradiations.

Finally, the final aperture was removed from the SEM column in order to expose the sample to the highest possible electron beam current. This did however make it more difficult to focus the image.

## 2.4 ELECTRICAL MEASUREMENT SYSTEM

All of the high frequency Capacitance-Voltage (C-V) and Current-Voltage (I-V) Measurements were performed on a modified version of the Hewlett Packard (HP) Model 4061A Semiconductor / Component Test System. The standard 4061A Test System consists of a 4275A Multi-frequency LCR Meter for AC impedance measurements, a 4140B pA/DC Voltage Source for current-voltage measurements, a switching subsystem to switch the device under

test between the two instruments and a 9836S HP 200 Series Computer with assorted software. Our modified system however used a HP 4192A Low Frequency Impedance Analyzer and a 9153 300 Series HP computer for the C-V measurements instead of the 4275A and the HP 200 Series Computer. The 9153 computer was also used to control the 4140B pA for the I-V measurements, while the switching subsystem was not even used. In addition, many changes needed to be made to the software in order to make it compatible to the new 4192A analyzer and the new 300 Series HP computer. Several other changes were also made to HFALL in order for the program to work on InP substrates and also allow for the storage and retrieval of data. This new version of HFALL was renamed HFCV92.

The modified BASIC program "HFCV92" needs an input of what kind of substrate and insulator is being used, the measurement frequency, the upper and lower bias limits, the gate area, the insulator thickness, and the substrate temperature. In order to avoid possible effects of charge injection from the substrate into the insulator on the interface state density at midgap, the C-V measurements were taken starting from inversion towards accumulation, since charge injection occurs only at voltages smaller than the flatband voltage [25]. From these input conditions the program calculates the following key parameters:

Cox : Capacitance of the Insulator Layer (F)  
 Cmin: Minimum MIS capacitance (F)  
 Vth : Threshold Voltage (V)  
 Cfb : Flat-band Capacitance (F)  
 Vfb : Flat-band Voltage (V)  
 Nsub: Substrate Impurity Concentration ( $\text{cm}^{-3}$ )

Cox is the maximum capacitance value of the high frequency C-V measurement given in units of capacitance per unit area. While Vth is defined by the following equation for an ideal capacitor:

$$V_{th} = V_{fb} + 2(\Phi_{if}) - \frac{A (Q_b)}{C_{ox}} \quad (1)$$

where:

A is the gate area ( $\text{cm}^2$ )  
 $\Phi_{if}$  is the fermi potential of the semiconductor given by:

$$\Phi_{if} = \pm \frac{k(T) \ln(N_{sub}/n_i)}{q} \quad (2)$$

where:

k is Boltzmann's constant ( $1.38 \times 10^{-23} \text{ J/K}$ )

T is the temperature (K)

q is the electron charge ( $1.602 \times 10^{-19} \text{ coulombs}$ )

$n_i$  is the intrinsic carrier substrate concentration



$Q_b$  is the charge per unit area in the MIS structure and is defined by:

$$Q_b = \pm \frac{N_{sub} (q) (E_o) (K_s)}{C_{smin}} \quad (3)$$

where:

$E_o$  is the permittivity of free space ( $8.854 \times 10^{-14}$  F/cm)  
 $K_s$  is the substrate dielectric constant  
 $C_{smin}$  is the minimum space charge capacitance  
and is defined by:

$$C_{smin} = \frac{(C_{min}) (C_{ox})}{C_{ox} - C_{min}} \quad (4)$$

$V_{fb}$  is determined by first calculating a value for  $C_{fb}$ . Then which ever bias voltage provides a measured capacitance nearest to the calculated value of  $C_{fb}$  is defined as  $V_{fb}$ . Where  $C_{fb}$  is defined by the following equation:

$$C_{fb} = \frac{(C_{ox}) (C_{sfb})}{C_{ox} + C_{sfb}} \quad (5)$$

where:

$C_{sfb}$  is the space charge capacitance at the flat condition and is defined as:

$$C_{sfb} = (2)^{1/2} \frac{(A) (E_o) (K_s)}{\text{Debye}} \quad (6)$$

where Debye is the Debye length defined as:

$$\text{Debye} = [2(k)(T)(E_0)(K_s)] / [(q^2)(N_{\text{sub}})] \quad (7)$$

The program will then plot the C-V curve on the screen and give the user the options of printing the C-V curve, storing the data in a file that is named by the user or both.

## CHAPTER 3. EXPERIMENTAL PROCEDURE

### 3.1 SUBSTRATE SPECIFICATIONS

The metal-insulator-semiconductor (MIS) capacitors were fabricated on both n-type and p-type InP liquid encapsulated Czochralski (LED) grown polished wafers. The undoped n-type wafers were of (100) orientation with carrier concentrations from  $4.0 \times 10^{15}$  to  $4.1 \times 10^{15} \text{ cm}^{-3}$ . While the p-type wafers were Zinc (Zn) doped wafers of (100) orientation and carrier concentrations of  $7 \times 10^{16} \text{ cm}^{-3}$ .

The metal-oxide-semiconductor (MOS) capacitors were fabricated using boron doped, p-type, silicon (Si) 3 inch diameter polished wafers. These wafers were grown by the Czochralski method and have a (100) orientation with impurity concentrations on the order of  $3.0 \times 10^{15} \text{ cm}^{-3}$ .

### 3.2 SUBSTRATE CLEANING

The first step in the processing of these InP based MIS devices was to perform a substrate degrease and initial cleaning that was evaluated by Biedenbender [31]. The InP substrate cleaning procedure began with a degreasing process consisting of a 5 minute soak in boiling trichloroethylene (TCE), followed by 5

minute soaks in acetone and then methonal, each with ultrasonic agitation. This removes the carbon based contamination on the substrate surface. The last step was a 5 minute deionized water (DI H<sub>2</sub>O) rinse. After degreasing, the rest of the substrate cleaning consisted of the following steps:

- (i) (1:1:4)12:1 (HCl:HF:DI H<sub>2</sub>O):H<sub>2</sub>O<sub>2</sub> for 30 sec.
- (ii) 10 wt % H<sub>3</sub>PO<sub>4</sub> in DI H<sub>2</sub>O for 3 min.
- (iii) DI H<sub>2</sub>O rinse for 5 min.
- (iv) 10 wt % HIO<sub>3</sub> in DI H<sub>2</sub>O for 5 min.
- (v) DI H<sub>2</sub>O rinse for 5 min.
- (vi) (1:1:4)12:1 (HCl:HF:DI H<sub>2</sub>O):H<sub>2</sub>O<sub>2</sub> for 15 sec.
- (vii) 10 wt % H<sub>3</sub>PO<sub>4</sub> in DI H<sub>2</sub>O for 15 sec.
- (viii) DI H<sub>2</sub>O rinse for 5 min.
- (ix) Blow dry with N<sub>2</sub>.

where:

HCl denotes hydrochloric acid  
HF denotes hydrofluoric acid  
H<sub>2</sub>O<sub>2</sub> denotes hydrogen peroxide  
H<sub>3</sub>PO<sub>4</sub> denotes phosphoric acid  
HIO<sub>3</sub> denotes iodic acid  
NH<sub>4</sub>OH denotes ammonia peroxide

The first two steps stripped the native oxide. This was done by first oxidizing the surface and then etching the oxide. After the native oxide was removed, 1000 Å of the InP substrate

was etched in step four to remove any polishing damage. Steps six and seven stripped any native oxide that might have formed during the  $\text{HIO}_3$  etch.

In addition to this initial cleaning of the InP substrate surfaces, another surface cleaning was required after the ohmic contact alloying step during device processing. This short cleaning procedure began with the same four degreasing steps used in the initial surface cleaning followed by the following steps:

- (i) (10:1) (HF:DI  $\text{H}_2\text{O}$ ) for 3 min.
- (ii) DI  $\text{H}_2\text{O}$  rinse for 5 min.
- (iii) 10 wt %  $\text{HIO}_3$  for 1 min.
- (iv) DI  $\text{H}_2\text{O}$  rinse for 5 min.
- (v) (10:1) (HF:DI  $\text{H}_2\text{O}$ ) for 3 min.
- (vi) DI  $\text{H}_2\text{O}$  rinse for 5 min.
- (vii) Blow dry with  $\text{N}_2$ .

The Si substrate cleaning procedure also began with the same degrease as above for the InP followed by these steps:

- (i) Hot soak in  $\text{H}_2\text{O}/\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$  solution for 15 min.
  - (a) 50ml of  $\text{NH}_4\text{OH}$  and 250ml of DI  $\text{H}_2\text{O}$  at  $70 \pm 5$  C.
  - (b) Add 50ml of  $\text{H}_2\text{O}_2$ .

- (c) Let bubble for 2 min before soaking wafers.
  
- (ii) DI H<sub>2</sub>O rinse for 5 min.
- (iii) (1:1) (HF:DI H<sub>2</sub>O) for 2 min.
- (iv) DI H<sub>2</sub>O rinse for 5 min.
- (v) Hot soak in H<sub>2</sub>O/H<sub>2</sub>O<sub>2</sub>/HCl solution for 15 min.
  - (a) 50ml of HCl and 200ml of DI H<sub>2</sub>O at 70±5 C.
  - (b) Add 50ml of H<sub>2</sub>O<sub>2</sub>.
  - (c) Let bubble for 2 min before soaking wafers.
  
- (vi) DI H<sub>2</sub>O rinse for 5 min.
- (vii) Blow dry with N<sub>2</sub>.

Step one oxidized the remaining organic contaminants on the substrate surface and also removed any heavy metals by forming complex amine groups with them. Then step three etched the native oxide. Finally step four removed any light alkali ions and also prevented displacement plating from the solution [34]. Therefore, this cleaning procedure removed residual, organic, ionic and atomic contamination from the Si surface.

### 3.3 OHMIC CONTACT FORMATION

An MIS capacitor consists of a metal gate electrode and a semiconductor separated by an insulating layer. However in order to make an electrical connection to the device, an ohmic contact is required and in this case it is on the backside of the semiconductor. By definition, an ohmic contact must have low resistance independent of polarity. A specific alloy or eutectic containing a dopant is used for a specific substrate and conductivity type. In this case, n-type InP, p-type InP and p-type Si substrates were used.

For the InP substrates, two different ohmic contacts were used. In the first case, which will be referred to as "Set A", the ohmic contacts were formed after the deposition of the insulating films. For the n-type InP substrates this consisted of a 900 Å layer of a gold-germanium (Au-Ge) eutectic (12 wt % Ge in Au) which was deposited first. Then 250 Å of nickel (Ni) was deposited second followed by an overlayer of Au 2000 Å thick. This trilayer of metal was then alloyed for 5 min in N<sub>2</sub> at 300 C.

For the p-type InP substrates in "Set A", the ohmic contacts were formed by the following procedure. First a 1600 Å layer of a gold-zinc (Au-Zn) eutectic was deposited followed by an overlayer of Au 2100 Å thick. This was followed by a 10 min alloy at 400 C in an N<sub>2</sub> ambient.

In the second case, where the ohmic contacts were formed on the n-type InP substrates before the film deposition, will be referred to as "Set B". Only 750 Å of Au-Ge eutectic (12 wt % Ge in Au) were deposited first. This was again followed by a 250 Å layer of Ni and then by a thinner 1600 Å overlayer of Au. This trilayer was also alloyed, however this time at a higher temperature of 400 C for 10 min in an N<sub>2</sub> ambient, because there were no insulating films to protect on the frontside. For the p-type InP substrates in "Set B", the same ohmic contacts were used as for "Set A".

There were several problems with "Set A" of the n-type InP samples and with the p-type Si samples, because the insulating films were already on the frontside of these samples during the formation of the ohmic contacts. More specifically, there was a thin native oxide films on the backside of the Set A InP samples that oxidized during the film deposition. And in the case of the Si samples, the SiO<sub>2</sub> layer grows on both sides of the wafer during the oxidation process. Therefore the backsides of both sets of samples had to be cleaned prior to the ohmic contact formation. This was where one of the problems set in, because an HF solution had to be used in order to strip the native oxide from the backside of the samples. The HF solution was applied to the backside with a cotton swab in order to keep it from attacking the oxide on the frontside. However some of the HF still managed to reach the edges and strip portions of the gate oxide on the frontside. The following procedure yielded the best



results for stripping the backside native oxide, protecting the frontside gate oxide and depositing the ohmic contact metals:

- (i) Spin on a layer of photoresist 1.0 to 1.5 micrometers thick onto the frontside of the samples.
- (ii) Bake the sample for 30 min at 110 C and then cool to room temperature.
- (iii) Strip the native oxide from the backside of the samples using (10:1) (DI H<sub>2</sub>O:HF) with a cotton swab until the backside shows a de-wetting effect.
- (iv) Rinse in DI H<sub>2</sub>O for 5 min and blow dry with N<sub>2</sub>.
- (v) Immediately deposit proper metals onto the backside for ohmic contacts.
  - (a) Make sure that the frontside oxide does not make contact with the deposition platen.
  - (b) Use a metal mask to leave an undeposited strip of semiconductor on the backside for resistivity measurements (See Figure 3.1).

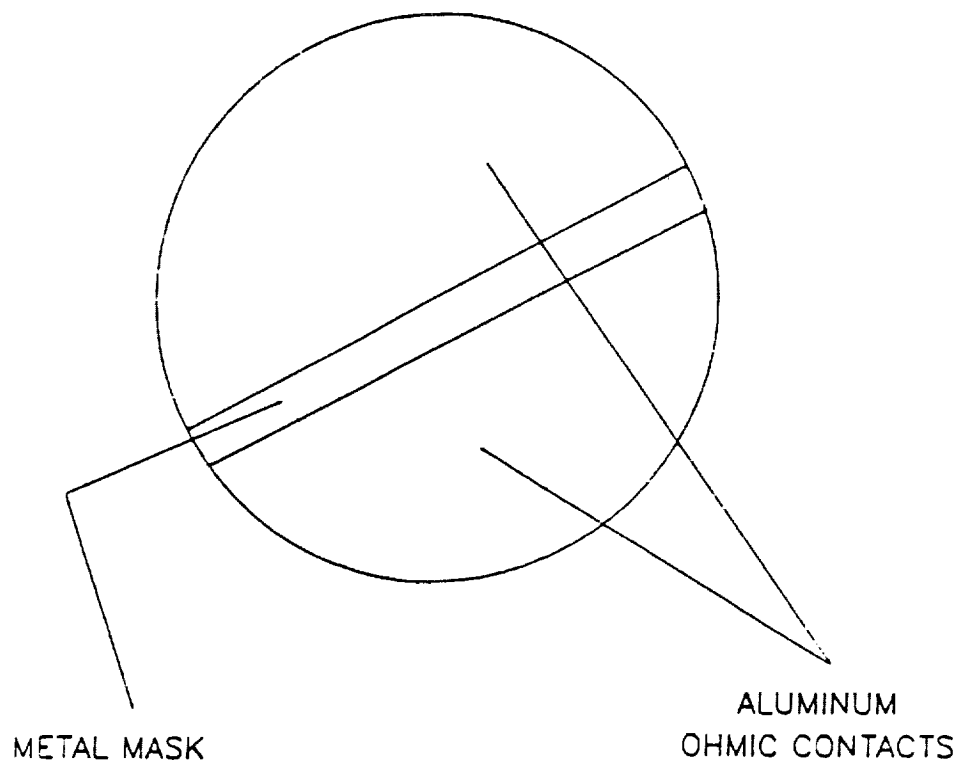


Figure 3.1 shows the shape of the shape of the ohmic contact metal deposition on the backside of the wafers.

- (vi) Check resistivity of ohmic contacts with an curve tracer.
- (vii) Strip the photo resist from the frontside by soaking the samples in Acetone for 5 min and then Methonal for 5 min.
- (viii) Rinse in DI H<sub>2</sub>O for 5 min and blow dry with N<sub>2</sub>.

Another procedure that was tried was to remove the photoresist prior to the ohmic contact metal deposition. However any incidental contact to the frontside during the loading and unloading of the samples into the deposition chamber caused defects to appear in the insulator.

Finally in the case of all of the p-type Si substrates, the ohmic contacts were formed after the growth of the thermal oxide. A single layer of aluminum (Al) 3000 Å thick was evaporated onto the backside of all the wafers followed by a 5 min alloy at 300 °C in N<sub>2</sub>.

### 3.4 INSULATOR DEPOSITIONS

All of the plasma enhanced chemical vapor depositions (PECVD) were performed in the Technics Planner Etch PE-IIA plasma system described in chapter 2. There were a total of six different groups of depositions performed. One group of depositions was performed at low frequency and five groups at high frequency. They will be described in the order that they were completed. The deposition procedure consists of seven parts which are described below.

First of all, since all of the gas lines are always purged and filled with  $N_2$  when not in use (See chapter 2, pages 5-6, i-xi). The first step prior to any depositions was to fill all of the gas lines one at a time with pure reactant gases (described in the procedure below). The following deposition procedure was followed for the first three groups of depositions. Steps i-vi describe the purification of the ammonia ( $NH_3$ ) lines:

#### I. AMMONIA LINE PURIFICATION

- (i) Evacuate deposition chamber by following procedure on page 3 of chapter 2.
- (ii)  $NH_3$  cylinder valve,  $NH_3$  regulator output back purge valves should already be closed. Turn the "Gas 1" flow switch on the front of the

deposition system to the on position. Then switch  $\text{NH}_3$  mass flow controller to the flow position, evacuating the  $\text{N}_2$  present in line.

- (iii) Allow the chamber pressure to reach below 100 mTorr, then turn flow-switch to off position.
- (iv) Open and close the  $\text{NH}_3$  regulator output valve, then switch the mass flow controller back to flow position. This allows the  $\text{N}_2$  in the regulator to be evacuated as well. Allow the chamber pressure to reach below 100 mTorr again then turn flow-switch to off position.
- (v) Open and close the  $\text{NH}_3$  cylinder valve, then open the regulator output valve to allow  $\text{NH}_3$  to fill the line. Next turn flow-switch to flow to evacuate the line to below 100 mTorr, then turn flow-switch to off position.
- (vi) Repeat step (v) two more times.

Prior to performing the deposition, the chamber was first cleaned of contaminants from any previous depositions. This is accomplished with a Freon-14 ( $\text{CF}_4$ ) plasma etch. The procedure is shown below:

## II. CF<sub>4</sub> PLASMA ETCH

- (i) Check that CF<sub>4</sub> regulator output valve is closed. Then evacuate the CF<sub>4</sub> line by turning the "Gas 2" flow switch on the front of the deposition system to the on position.
- (ii) Allow the chamber pressure to reach below 100 mTorr, then turn off the "Gas 2" flow switch.
- (iii) Open the CF<sub>4</sub> cylinder valve, then open the CF<sub>4</sub> regulator output valve allowing CF<sub>4</sub> to fill the line.
- (iv) Turn the "Gas 2" flow switch to the on position and slowly increase the CF<sub>4</sub> flow until the chamber pressure reaches 200 mTorr. Let this flow rate and pressure stabilize for 5 minutes.
- (v) Turn on and set the appropriate RF power. Let the CF<sub>4</sub> plasma burn for 5 minutes.
  - (a) For low frequency depositions at 30 kHz the RF power is set at 100 Watts (W).
  - (b) For high frequency depositions at 13.56 MHz the RF power was set at 150 W.

- (vi) Turn of the RF power, turn "Gas 2" flow switch to off, close the CF<sub>4</sub> regulator output valve and close the CF<sub>4</sub> cylinder valve in that order.

There was still one more step before the deposition of the films. This was the N<sub>2</sub> plasma burn. This step prevented any fluorine contamination of the films from the previous CF<sub>4</sub> etch. This step is shown below:

### III. N<sub>2</sub> PLASMA BURN

- (i) Open the N<sub>2</sub> cylinder valve and the N<sub>2</sub> regulator output valve. Then turn the N<sub>2</sub> flow-switch on the mass flow controller to the flow position (the "Gas 1" flow-switch on the front of the deposition system should already be on).
- (ii) Set the N<sub>2</sub> mass flow controller to full flow (10.0 sccm) for 2 minutes allowing the N<sub>2</sub> to flow through the lines. Then set the N<sub>2</sub> flow rate to 30 sccm.
- (iii) Turn on the RF power igniting the plasma and set the it to the appropriate power. Let the plasma burn for 5 minutes to burn off all of the fluorine.

- (a) For low frequency depositions at 30 kHz  
the RF power is set at 100 Watts (W).
- (b) For high frequency depositions at 13.56  
MHz the RF power was set at 150 W.
- (iv) Before turning off the RF power, set the power  
to what is desired for the film deposition.
  - (a) For low frequency depositions at 30 kHz  
the RF power is set at 30 W.
  - (b) For high frequency depositions at 13.56  
MHz the RF power was set at 30 W.
- (v) Turn off the RF power but keep the N<sub>2</sub> flowing  
at 30 sccm for an additional 5 minutes. Then  
turn off the N<sub>2</sub> flow-switch.

The next step was the loading of the samples into the deposition chamber. The samples were placed about the exhaust port in the center of the lower electrode. The trick was to find a way to close the chamber and evacuate it without causing the samples to shift. The loading procedure is shown below:



#### IV. SAMPLE LOADING

- (i) Close the throttle valve by turning the control switch on the MKS 262A exhaust valve controller to the "manual close" position. Close the solenoid valve on the front of the deposition system by switching it to the off closed position.
- (ii) Vent the deposition chamber by flipping the vent switch on the front of the deposition chamber to the open position. The chamber pressure should read 1.0 Torr (even though the chamber is at atmosphere)
- (iii) Open the deposition chamber and open the solenoid valve to the chamber (set in open position)
- (iv) Load the samples and gently close the deposition chamber.
- (v) Open the throttle valve by turning the control switch to "manual open" position. The chamber pressure should begin dropping immediately.

The next step was the N<sub>2</sub> bakeout to outgas the chamber by using the heater in the lower electrode, shown below:

#### V. N<sub>2</sub> BAKEOUT

- (i) Turn the N<sub>2</sub> flow-switch to the flow position and set the flow rate to 30 sccm. (No plasma is used)
- (ii) Turn on the lower electrode heater in the chamber by setting the Warlow temperature controller to 300 C. Let the chamber bakeout for one hour.

The last step before the deposition was the purification of the silane (SiH<sub>4</sub>) lines by evacuating the N<sub>2</sub> present in the lines and filling them with SiH<sub>4</sub>. This step was performed last in order to have silane in the lines for as short a period as possible. This step is shown below:

#### VI. SILANE LINE PURIFICATION

- (i) The "Gas 1" flow switch on the front of the deposition system should already be in the on position. Switch SiH<sub>4</sub> mass flow controller to

the flow position, evacuating the  $N_2$  present in line.

- (ii) Allow the chamber pressure to reach below 100 mTorr, then turn the  $SiH_4$  flow-switch to off position.
- (iii) Open and close the  $SiH_4$  regulator output valve, then switch the mass flow controller back to flow position. This allows the  $N_2$  in the regulator to be evacuated as well. Allow the chamber pressure to reach below 100 mTorr again then turn  $SiH_4$  flow-switch to the off position.
- (iv) Open and close the  $SiH_4$  cylinder valve keeping the pressure in the  $SiH_4$  regulator at very low pressure ( $< 10$  psi.). Then open the regulator output valve slowly to allow  $SiH_4$  to fill the line. Next turn the  $SiH_4$  flow-switch to flow position to evacuate the line to below 100 mTorr, then turn flow-switch to back to the off position.
- (v) Repeat step (v) two more times to make sure there is pure silane in the line.

The final step is the actual deposition of the insulating films. The deposition conditions have been investigated by Valco [35,36] and Young [37], and this data was used as a starting point. The silicon nitride deposition procedure for sample Groups I,II and III is described below:

#### VIIA. SILICON NITRIDE FILM DEPOSITION

- (i) The temperature of the lower electrode should already be set at 300 C. If not, wait until temperature stabilizes at the point.
- (ii) Turn the throttle valve control switch on the MKS 262A Exhaust Valve Controller to the "auto" position, then set the chamber pressure to be controlled at 500 mTorr. Set the phase knob to 3.0 and the gain knob to 20.0. This allows for the quickest control of the chamber pressure under these conditions.
- (iii) Turn on flow-switches and set flow rates of reactant gases to appropriate values. Allow flow rates and chamber pressure to stabilize for 5 minutes. These flow rates were used for all of the depositions of Groups I, II and III.

- (a) Set  $N_2$  flow rate to 40.0 sccm.
  - (b) Set  $NH_3$  flow rate to 40.0 sccm.
  - (c) Set  $SiH_4$  flow rate to 9.0 sccm.
- (iv) Turn on the appropriate RF power source (30 kHz low frequency or 13.56 MHz high frequency) to ignite the plasma. The power must already have been set following the  $N_2$  plasma burn in section III.
- (vii) Let deposition run for appropriate time.
- (a) Group I:  
Deposition #1 time was 5.0 minutes.  
Deposition #2 time was 6.0 minutes.
  - (b) Group II  
Deposition time was 4.0 minutes.
  - (d) Group III  
Deposition #1 time was 4.0 minutes.  
Deposition #2 time was 4.0 minutes.
- (viii) Turn off the RF power source, turn the  $SiH_4$  and the  $NH_3$  flow-switches to the off positions. Allowing only the  $N_2$  to flow for a minute. Then turn off the  $N_2$  flow-switch.
- (ix) Vent the deposition chamber by flipping the vent switch on the front of the deposition chamber to the open position. As soon as the chamber pressure reaches above 1.0 Torr, flip the vent switch back to the closed position and

let the chamber evacuate to below 100 mTorr. Repeat this venting and evacuating step two more times, then leave the vent switch open. Allow the lower electrode temperature to cool to below 200 C before opening the chamber to unload the samples.

- (x) If this was the last deposition, then follow the N<sub>2</sub> purge and fill procedure in chapter 2 on page 8.

The last three groups of samples were all deposited at high frequency (13.56 MHz) and all had a phosphorus rich layer at the insulator/semiconductor interface. This means that during the loading of the samples a red amorphous phosphorus source was also loaded into the chamber. The phosphorus was contained in a ceramic boat with an aluminum top that had small holes for the phosphorus to escape. The substrate samples were placed between the phosphorus source and the exhaust port (See Figure 3.2). This phosphorus rich interface was investigated by Young [38], and he discovered that it improves the interface properties and reduces the interface state density. This high frequency silicon nitride and silicon dioxide deposition procedure is described below follows immediately after section V (N<sub>2</sub> Bakeout) before section VI (Silane Line Purification):

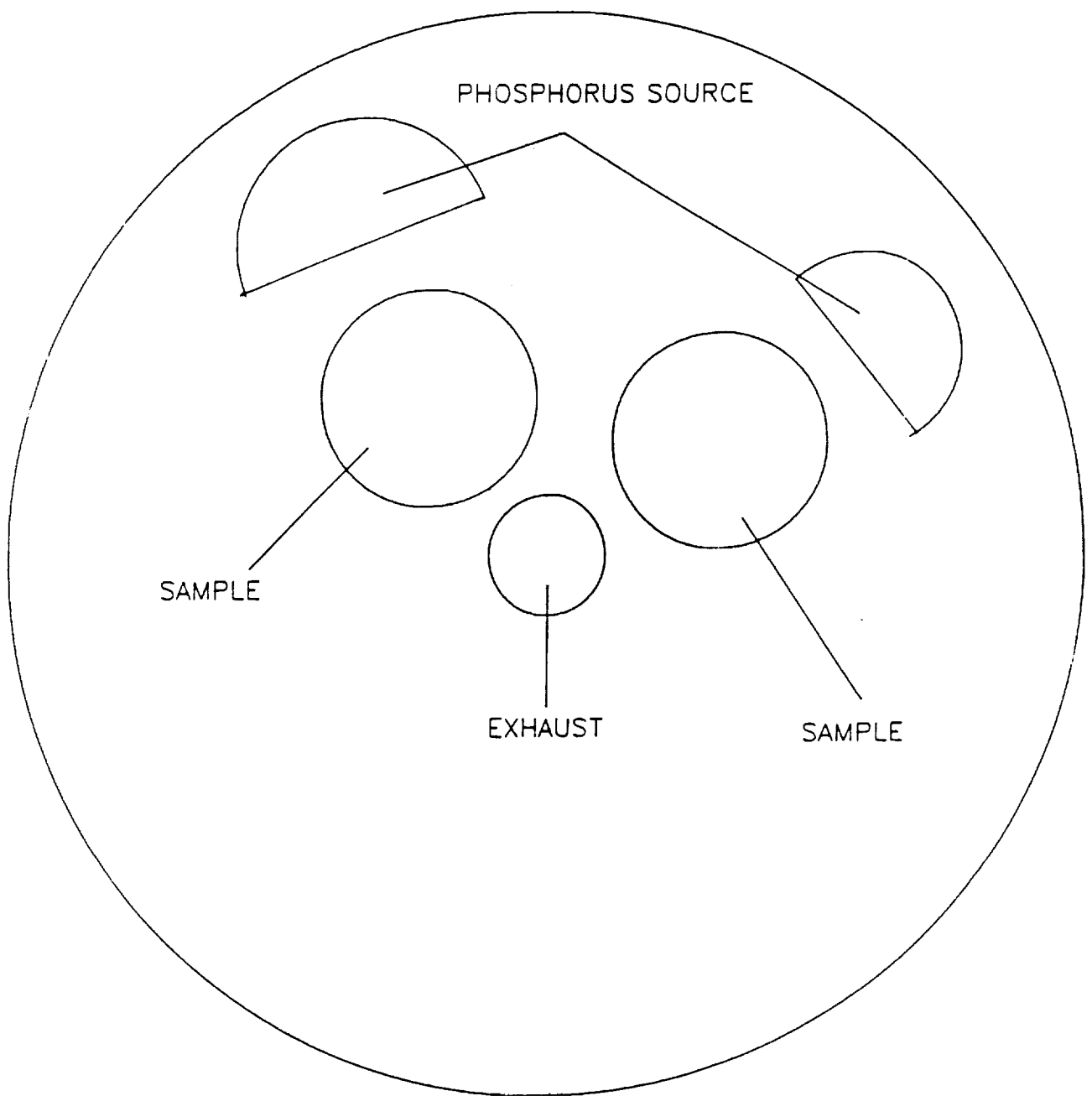


Figure 3.2 shows the positions of the samples in the deposition chamber for the phosphorus rich films.

## VIIB. PHOSPHORUS RICH FILM DEPOSITION

- (i) Set the temperature of the lower electrode to the appropriate value. Wait until the temperature stabilizes at this point before depositing films.
  - (a) For silicon nitride depositions (Groups IV and V) the temperature should be set at 300 C.
  - (b) For silicon dioxide depositions (Group VI) the temperature should be set at 275 C.
- (ii) Turn the throttle valve control switch on the MKS 262A Exhaust Valve Controller to the "auto" position, then set the appropriate chamber pressure to be controlled. Set the phase knob to 8.0 and the gain knob to 5.0.
  - (a) For silicon nitride depositions (Groups IV and V) the chamber pressure should be set at 500 mTorr.
  - (b) For silicon dioxide depositions (Group VI) the chamber pressure should be set at 800 mTorr.



- (iii) Turn the  $N_2$  flow-switch to the flow position and set the flow rate to 20 sccm.
- (iv) Turn on the high frequency RF power generator and set it at 30 W for 5 minutes. This step deposits a thin layer of phosphorus onto the substrate surface.
- (v) Turn off the RF power and increase the  $N_2$  flow rate to 30 sccm. Let the samples bake for 5 minutes before tuning of the  $N_2$  flow.
- (vi) Switch the "T" valve in the  $N_2$  gas line from  $N_2$  to the nitrous oxide ( $N_2O$ ) gas line.
- (vii) Switch  $N_2O$  mass flow controller to the flow position, evacuating the  $N_2$  present in line.
- (viii) Allow the chamber pressure to reach below 100 mTorr, then turn  $N_2O$  flow-switch to off position.
- (ix) Open and close the  $N_2O$  regulator output valve, then switch the mass flow controller back to flow position. This allows the  $N_2$  in the regulator to be evacuated as well. Allow the chamber pressure to reach below 100 mTorr again then turn  $N_2O$  flow-switch to off position.

- (x) Open and close the N<sub>2</sub>O cylinder valve, then open the regulator output valve to allow N<sub>2</sub>O to fill the line. Next turn N<sub>2</sub>O flow-switch to flow to evacuate the line to below 100 mTorr, then turn flow-switch to off position.
- (xi) Repeat step (x) two more times. This purifies the N<sub>2</sub>O gas line.
- (xii) Turn the N<sub>2</sub>O flow-switch to the flow position and set the flow rate to 30 sccm.
- (xiii) Turn on the high frequency RF power generator and set it at 30 W for 5 minutes. This step oxidizes the phosphorus and reduces the thickness of the already deposited phosphorus layer.
- (xiv) Go to section VI and follow the procedure for the purification of the silane line.
- (xv) Turn the throttle valve control switch on the MKS 262A Exhaust Valve Controller to the "auto" position, then set the appropriate chamber pressure to be controlled. Set the phase knob to 3.0 and the gain knob to 20.0.

(xvi) Turn on flow-switches and set flow rates of reactant gases to appropriate values. Allow flow rates and chamber pressure to stabilize for 5 minutes.

(a) Group IV:

Deposition #1: N<sub>2</sub> flow rate 30.0 sccm.  
NH<sub>3</sub> flow rate 30.0 sccm.  
SiH<sub>4</sub> flow rate 15.0 sccm.

Deposition #2: N<sub>2</sub> flow rate 40.0 sccm.  
NH<sub>3</sub> flow rate 40.0 sccm.  
SiH<sub>4</sub> flow rate 9.0 sccm.

Deposition #3: N<sub>2</sub> flow rate 40.0 sccm.  
NH<sub>3</sub> flow rate 40.0 sccm.  
SiH<sub>4</sub> flow rate 12.0 sccm.

Deposition #4: N<sub>2</sub> flow rate 40.0 sccm.  
NH<sub>3</sub> flow rate 40.0 sccm.  
SiH<sub>4</sub> flow rate 14.0 sccm.

Deposition #5: N<sub>2</sub> flow rate 40.0 sccm.  
NH<sub>3</sub> flow rate 40.0 sccm.  
SiH<sub>4</sub> flow rate 15.0 sccm.

(b)           Group V:

Deposition #1:    $\text{N}_2$  flow rate 40.0 sccm.  
                   $\text{NH}_3$  flow rate 40.0 sccm.  
                   $\text{SiH}_4$  flow rate 15.0 sccm.

Deposition #2:    $\text{N}_2$  flow rate 40.0 sccm.  
                   $\text{NH}_3$  flow rate 40.0 sccm.  
                   $\text{SiH}_4$  flow rate 15.0 sccm.

(c)           Group VI:

Deposition #1:    $\text{N}_2\text{O}$  flow rate 55.0 sccm.  
                   $\text{SiH}_4$  flow rate 17.4 sccm.

(xvii) Turn on the 13.56 MHz high frequency RF power source to ignite the plasma. The power must already have been set following the  $\text{N}_2$  plasma burn in section III.

(xviii) Let all depositions run for 5.0 min  
(Groups IV-VI).

(xix) Turn off the RF power source, turn the  $\text{SiH}_4$  and the  $\text{NH}_3$  or  $\text{N}_2\text{O}$  flow-switches to the off positions.

(xx) Vent the deposition chamber by flipping the vent switch on the front of the deposition

chamber to the open position. As soon as the chamber pressure reaches above 1.0 Torr, flip the vent switch back to the closed position and let the chamber evacuate to below 100 mTorr. Repeat this venting and evacuating step two more times, then leave the vent switch open. Allow the lower electrode temperature to cool to below 200 C before opening the chamber to unload the samples.

- (xxi) If this was the last deposition, then follow the N<sub>2</sub> purge and fill procedure in chapter 2 on page 8.

The deposition conditions for the PECVD silicon dioxide films with a phosphorus rich interface have been optimized by Young [37]. Therefore these conditions were used for the deposition performed in Group VI above.

Therefore a total of six groups of depositions were performed and their procedures have been described above. The n-type and p-type InP substrates in Group III had their ohmic contacts formed after the insulator deposition. This means that they are part of InP Set A. While the n-type and p-type substrates in Groups V and VI had their ohmic contacts formed prior to the insulator deposition step, which means that they are part of Set B. Refer section 3.3 on ohmic contact formation. (See Table 3.1 for a listing of the different sample groups.)

TABLE 3.1

DEPOSITION GROUPS

SAMPLE	f	PHOS RICH	FILM TYPE	N <sub>2</sub> sccm	NH <sub>3</sub> sccm	SiH <sub>4</sub> sccm	TIME min	TEMP (C)	PRES mTORR
--------	---	--------------	--------------	------------------------	-------------------------	--------------------------	-------------	-------------	---------------

GROUP I

Dep #1: 4 p-Si	LF	NO	SiN	40	40	9	5	500	300
Dep #2: 4 p-Si	LF	NO	SiN	40	40	9	6	500	300

GROUP II

Dep #1: 2 p-Si	HF	NO	SiN	40	40	9	4	500	300
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GROUP III

Dep #1: 2 p-Si 2 n-InP 2 p-InP	HF	NO	SiN	40	40	9	4	500	300
Dep #2: 2 p-Si 2 n-InP 1 p-InP	HF	NO	SiN	40	40	9	4	500	300

TABLE 3.1 (continued)

SAMPLE	f	PHOS RICH	FILM TYPE	N <sub>2</sub> sccm	NH <sub>3</sub> sccm	SiH <sub>4</sub> sccm	TIME min	TEMP (C)	PRES mTORR
--------	---	--------------	--------------	------------------------	-------------------------	--------------------------	-------------	-------------	---------------

GROUP IV

Dep #1: 1 p-Si	HF	YES	SiN	40	40	9	5	500	300
Dep #2: 1 p-Si	HF	YES	SiN	30	30	15	5	500	300
Dep #3: 1 p-Si	HF	YES	SiN	40	40	12	5	500	300
Dep #4: 1 p-Si	HF	YES	SiN	40	40	14	5	500	300
Dep #5: 1 p-Si	HF	YES	SiN	40	40	15	5	500	300

GROUP V

Dep #1: 1 p-Si 1 n-InP 1 p-InP	HF	YES	SiN	40	40	15	5	500	300
Dep #2: 1 p-Si 1 n-InP 2 p-InP	HF	YES	SiN	40	40	15	5	500	300

GROUP VI

				<u>N<sub>2</sub>O</u> <u>sccm</u>					
Dep #1: 1 p-Si 1 n-InP	HF	YES	SiO <sub>2</sub>	55	0	17.4	5	800	275

Table 3.1 describes each of the deposition groups.

Where LF and HF denote low and high frequency respectively.

### 3.5 THERMAL PROCESSING

In the case of the p-type Si substrates, the initial clean was immediately followed by the growth of the silicon dioxide insulator. A dry thermal oxidation was performed in an open ended furnace tube. The  $O_2$  flow rate was 500 sccm at a furnace temperature of 900 C for 9.0 hours. The oxidation was succeeded by a 15 minute  $N_2$  anneal at the same temperature with 500 sccm of  $N_2$  flowing. This sample of thermal silicon dioxide on Si will now be referred to as Group VII.

In addition, this same furnace tube was used to perform a post-deposition anneal of one of the n-type InP Group V samples. The new PECVD phosphorous rich silicon nitride film was annealed in an  $H_2/N_2$  ambient for 15 minutes at 400 C. The gas ratio in the furnace was (2:1) ( $N_2:H_2$ ) with an  $H_2$  flow rate of 1000 sccm. This annealed sample will now be referred to as Group VIII.

Finally, both PECVD phosphorous rich silicon nitride on n-type InP samples from Groups V and VIII were  $H_2/N_2$  annealed after the electron-beam irradiations were performed. The post-irradiation anneals were performed in the same furnace tube at 400 C for 15 minutes with 2000 sccm of  $N_2$  and 1000 sccm of  $H_2$  flowing.



### 3.6 GATE METALIZATION

The final processing step for the samples was to deposit a metal gate to form the MOS and MIS capacitors. All of the samples from deposition Groups III and V-VIII only, will have the gate metalization step performed. The deposition groups containing only Si substrates have been excluded. Aluminum dots 0.2 cm in diameter and 1000 Å thick were electron-beam deposited onto the insulator using a dot shadow mask. This gate metal thickness was chosen as thin as possible so as to not appreciably reduce the incident electron-beam energy while thick enough to support the use of two probes for electrical measurements. The absorption of electron-beam energy in these 1000 Å aluminum gate electrodes was estimated to be less than 10 % ,therefore negligible and was not a factor [2,3,38].

### 3.7 ELECTRON-BEAM IRRADIATION AND CHARACTERIZATION

All of the samples were first tested to make sure they were good MIS capacitors. This was done by taking both I-V and C-V measurements of all of the devices. A record was kept of all of the good C-V dots which would be irradiated.

The samples were then cleaved into small pieces so they would be easier to work with and fit more easily into the SEM. A sample with several good C-V dots was then placed onto the Mini-

Probe stage in the SEM chamber which is set perpendicular to the electron beam. Two of the four probe tips were then lowered onto the edge of one of the good MIS capacitors. The other two probe tips were lowered onto the aluminum stage which was making electrical contact to the ohmic contact on the backside of the sample. In addition, a thermocouple lead was attached to the corner of the small sample near the dot with the probes on it (See Figure 3.3).

In order to take C-V measurements of the sample while it is inside the SEM chamber, the two probes on the aluminum C-V dot were connected to pin #7 and pin #9 of the 25 pin terminal board on the SEM chamber door, which in turn were connected (through a special cable, described in Section 2.4) to the high current ( $H_{CUR}$ ) and high potential ( $H_{POT}$ ) terminals on the 4192A LF Impedance Analyzer respectively. The two probes touching the aluminum stage were connected to pins #11 and #23 (of the terminal board) which in turn were connected to the low potential ( $L_{POT}$ ) and low current ( $L_{CUR}$ ) terminals on the 4192A respectively.

In order to properly irradiate the sample in the SEM, the front and back side of the sample had to be grounded to prevent charging of the samples surface. This was accomplished by connecting the coaxial cables from pin #7 and pin #23 to the input terminal of the SEM Specimen Current Amplifier (leaving the other two pins disconnected), which not only displayed the specimen current but served as a ground as well.

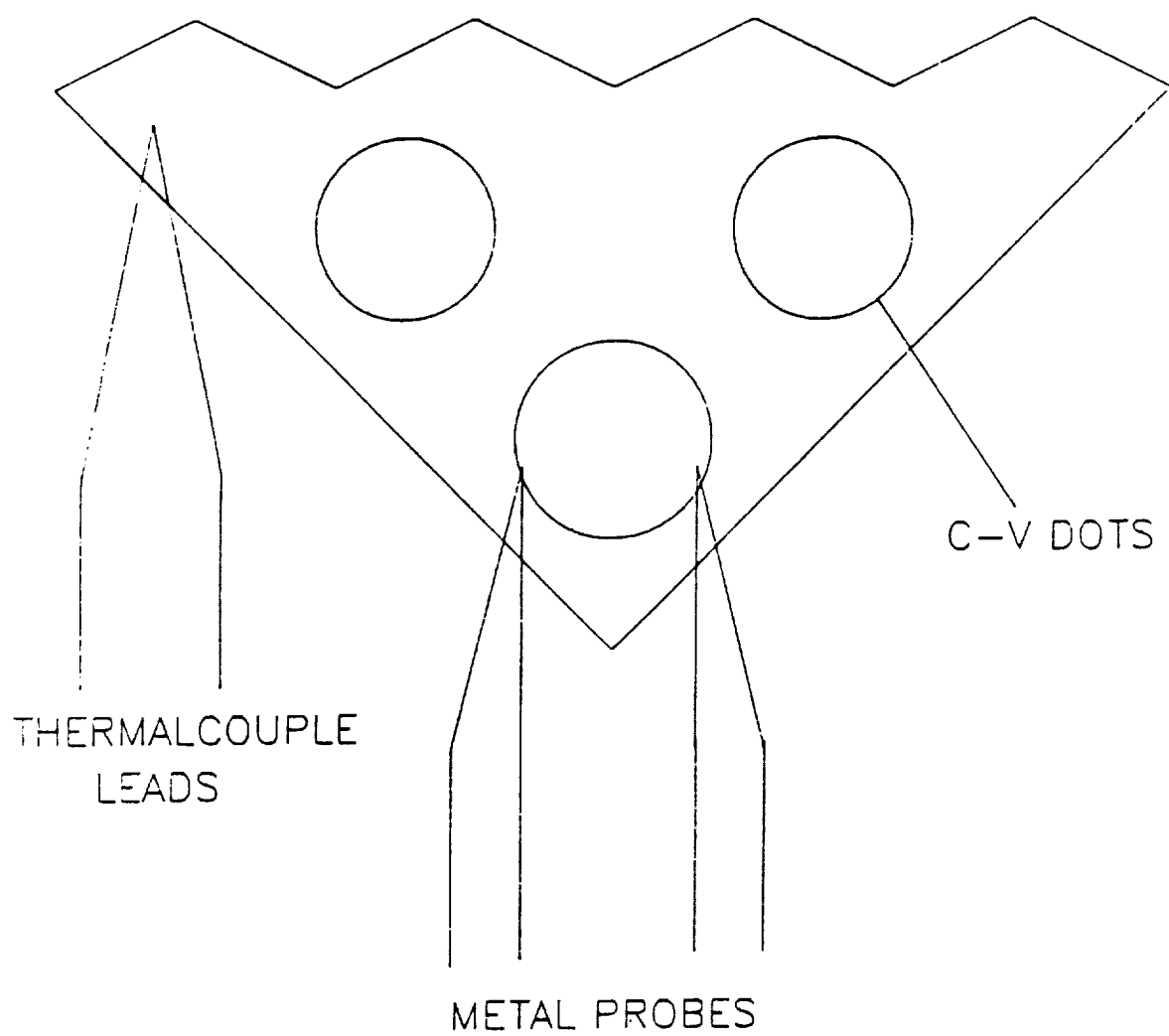


Figure 3.3 shows the position of the metal probes and the thermocouple on the sample in the SEM chamber.

The first step was to focus the SEM beam on a test sample, so that there was no initial damage caused to a good C-V dot during the focusing procedure. This step is shown below:

#### I. FOCUS TEST SAMPLE

- (i) Place an old test sample on SEM stage and make electrical contact to all four probes. Then connect pins #7 and #23 to the Specimen Current Amplifier.
- (ii) Evacuate the SEM chamber by pressing Stage 2 button on the column base and wait for the HT Ready Light to turn on. This means the chamber is sufficiently evacuated and the electron beam is ready to be turn on.
- (iii) Set electron beam energy to 20 keV.
- (iv) Push HT button to turn on SEM.
- (v) Turn the filament current slowly up to 2.4 Amperes (A) for optimum imaging.
- (vi) Find and focus the image of the MIS device with the probes connected to it.

- (vii) Turn off filament current and turn off HT button. Then wait 30 sec before venting the specimen chamber.

Now that the SEM is focused, a good sample can be placed into the specimen chamber to begin the irradiation experiments. However, care must still be taken so as not to cause any unnecessary irradiation of the C-V dot being tested. The following was found to be best procedure for irradiating and characterizing the samples:

## II. SAMPLE DAMAGE AND TESTING

- (i) Place sample on SEM stage and make electrical contact to all four probes. Then connect pins #7 and #23 to the Specimen Current Amplifier.
- (ii) Evacuate the SEM chamber and wait for the HT Ready Light to turn on again.
- (iii) Set electron beam energy to 2 keV, because this energy will not cause any damage to the sample.
- (iv) Push HT button to turn on SEM.
- (v) Turn the filament current slowly up to 2.4 A.

- (vi) Find and focus the image of the MIS device with the probes connected to it and center it in the middle of the screen. Then magnify the image until the edges of the dot are the size of the screen. This allows for the greatest concentration of electrons to hit the sample and not damage to many other devices.
- (vii) Turn off filament current and turn off HT button.
- (viii) Record the coordinates of the x and y-axis on the outside of the chamber door. Then move the stage so that the e-beam will be sufficiently away from the dot under test.
- (ix) Turn on the HT button and slowly increase the filament current to 2.4 A again.
- (x) Adjust the x,y coordinates again until there is another dot in the middle of the screen. Record these coordinates as well so that this dot can be re-used.
- (xi) Set the electron-beam energy to the desired energy for the experiment and set the desired specimen current as well. Then turn off the filament current only.

- (xii) Take an initial C-V measurement.
  - (a) Disconnect cables #7 and #23 from the Specimen Current Amplifier and connect them to the H<sub>CUR</sub> and H<sub>POT</sub> terminals on the 4192A LF Impedance Analyzer respectively. Then connect cables #11 and #23 to the L<sub>POT</sub> and L<sub>CUR</sub> terminals on the 4192A respectively.
  - (b) Run program "HFCV92" to take initial C-V measurement
- (xiii) Disconnect all cables from the 4192A and reconnect cables #7 and #23 to the Specimen Current Amplifier.
- (xiv) Now move the x, y coordinates to their original setting for the sample under test.
- (xv) Turn the filament current slowly up to 2.4 A, and irradiate the sample for the desired time period.
- (xvi) Turn off the filament current and turn off the HT button.

(xvii) Quickly disconnect cables #7 and #23 from the Specimen Current Amplifier and connect all four cables to their proper terminals on the 4192A Impedance Analyzer.

(xviii) Run program "HFCV92" to take a C-V measurement.

The low electron-beam energy of 2 keV was used to find the actual sample being tested, because it was found that this beam energy did not cause any noticeable damage to the device. However an initial C-V measurement is taken after this short 2 keV irradiation as a precaution.

In addition, the irradiation conditions for beam energy and specimen current were set on a different dot (away from the sample dot) instead of trying to set the correct specimen current on the test dot. This would create a problem of not knowing how long the dot was actually irradiated at the specific current. This means that the dot with the probes on it should be visible on the screen during the actual irradiation.

Once the irradiation period was over and the filament current was off, the coaxial cables were disconnected as quickly as possible from the specimen current amplifier and the proper connections were made to the impedance analyzer. Furthermore, the substrate temperature was monitored both during and after irradiations and the C-V measurement were not be started until



the substrate temperature had returned to its initial room temperature value. This way no temperature effects were recorded by the C-V measurement, but only the irradiation damage. Finally the time between the irradiation and the first C-V measurement had no effect on the C-V data.

A set of 5 to 10 high frequency (1 MHz) C-V measurements were taken prior to irradiation using the four probe measurement system. The exposures were made by raster scanning of the electron beam over an area larger than the Al dot for a desired dose ( $\text{C}/\text{cm}^2$ ) and beam energy (keV). The irradiation was followed by another set of 5 to 10 C-V measurements. This sequence was continued for total exposures of  $10^{-7}$ ,  $10^{-6}$ ,  $10^{-5}$ ,  $10^{-4}$  and  $10^{-3}$   $\text{C}/\text{cm}^2$  with a constant beam energy. This procedure was repeated for beam energies of 5, 10, 20, 30 and 40 keV, using a new Al dot for each energy.

Both PECVD phosphorus rich silicon nitride samples from Group V and VIII were  $\text{H}_2/\text{N}_2$  annealed after the irradiations were performed. A final set of C-V measurements was taken following the  $\text{H}_2/\text{N}_2$  anneal.

## CHAPTER 4. EXPERIMENTAL RESULTS

### 4.1 ELLIPSOMETRY RESULTS

The thermal silicon dioxide, PECVD silicon nitride and PECVD silicon dioxide films were characterized by the Gaertner L611A Ellipsometry system described in Section 2.2. The results of these ellipsometry measurements are shown in Table 4.1. The information obtained from these measurements was used to optimize the deposition conditions and obtain index of refraction values as close as possible to those in Table 2.3. This was accomplished by subjecting the films to variations in the deposition times and flow rates of the reactant gases as described in Section 3.4.

The non-phosphorus rich PECVD silicon nitride films in Groups I, II and III had the most uniform films over the entire wafer. The maximum variation in the film thickness between the center and the edge of the wafer was only a 10 to 20 Å. However, this was only true for one of the samples in the first deposition of Group III, one of the p-type InP samples. For the rest of the samples in this deposition, the films were very cloudy and not uniform. These bad films were stripped away using the CF<sub>4</sub> Plasma Etch described in Section 3.4-II, then subjected to another initial cleaning. These same substrates were then re-used in the second deposition of Group III, which turned out to be much more uniform.

TABLE 4.1

ELLIPSOMETRY RESULTS

Sample Tested	Average Film Thickness (Å)	Average Index of Refraction ( $N_f$ )	Average Deposition Rate (Å/min)
---------------	----------------------------	---------------------------------------	---------------------------------

GROUP I

Dep #1: (p-Si)	636	1.926	127
Dep #2: (p-Si)	969	1.936	161

GROUP II

Dep #1: (p-Si)	548	1.935	137
-------------------	-----	-------	-----

GROUP III

Dep #1: (p-Si)	701	1.932	175
Dep#2: (p-Si)	555	1.893	139
(n-InP)	530	1.906	133
(p-InP)	485	1.875	121

Table 4.1 shows the data obtained from the ellipsometry measurements of each deposition group.

TABLE 4.1 (Continued)

Sample Tested	Average Film Thickness (Å)	Average Index of Refraction ( $N_f$ )	Average Deposition Rate (Å/min)
---------------	----------------------------	---------------------------------------	---------------------------------

GROUP IV

Dep #1: (p-Si)	509	1.878	102
Dep #2: (p-Si)	654	2.194	131
Dep #3: (p-Si)	712	1.901	142
Dep #4: (p-Si)	821	1.965	164
Dep #5: (p-Si)	931	1.998	185

GROUP V

Dep #1: (p-Si)	926	1.997	185
(n-InP)	928	1.995	186
Dep #2: (n-InP)	892	1.982	178
(p-InP)	873	2.036	175

GROUP VI

Dep #1: (p-Si)	1000	1.453	200
(n-InP)	1477	1.485	295

GROUP VII

Oxidation #1:			<u>Oxidation Rate</u>
(p-Si)	850	1.423	94 Å/Hr.

In addition, the indices of refraction for the first three groups of depositions were all very close to the desired value for silicon nitride films of 2.05. For this reason the deposition parameters remained unchanged for these non-phosphorus rich film depositions.

The next three groups of depositions all had a phosphorus rich region at the insulator/semiconductor interface. This may have been the reason for the low index of refraction in the first deposition of Group IV, even though no changes were made to the deposition conditions from the previous group. Therefore an attempt was made to increase the refractive index in the next deposition.

It has been well documented that the refractive index of PECVD silicon nitride films varies linearly with the silicon to nitrogen ratio in the film [20, 39]. This means that in order to increase the index of refraction, the  $\text{SiH}_4$  gas flow rate must be increased or the  $\text{N}_2$  and  $\text{NH}_3$  gas flow rates must be decreased. In deposition #2 of Group IV, both of these measures were taken and as a result the refractive index was too high. It took five depositions, adjusting the  $\text{SiH}_4$  flow rate each time, to get the desired index of refraction. Once the deposition conditions were optimized, they remained unchanged for the Group V depositions. In addition, all of the Group IV and V films were very uniform.

The PECVD phosphorus rich silicon dioxide films deposited in Group VI were not as uniform as the silicon nitride films. There were differences of 100 to 300 Å between the center and the outer edge of the wafer. But since the minimum thickness was over 800 Å, this is still acceptable. The large difference the average film thickness between the Si and the InP substrates was due to the position of the samples in the deposition chamber. The InP sample was placed between the phosphorus source and the exhaust port but the Si sample was not. The refractive index of these films however, was very close to the desired value for silicon dioxide films of 1.46. The same is true of the thermally oxidized silicon dioxide sample in Group VII.

#### 4.2 ELECTRICAL CHARACTERIZATION RESULTS

MOS and MIS capacitors fabricated from the thermal silicon dioxide and PECVD silicon nitride and silicon dioxide films respectively, were electrically characterized by a modified version of the Hewlett Packard Model 4061A Semiconductor / Component Test System described in Section 2.4. High Frequency C-V measurements and I-V measurements were taken of the devices that were fabricated using the insulating films from Deposition Groups III, and V- VIII only. These measurements were used to determine which of the deposition groups yielded quality MOS and MIS capacitor devices. The results of these measurements are shown in Table 4.2.

TABLE 4.2

CAPACITOR YIELD

DEPOSITION GROUP	TYPE AND SUBSTRATE	DEVICE	CAPACITOR QUALITY
III	p-Si	MIS	BAD
III	n-InP	MIS	BAD
III	p-InP	MIS	BAD
V	p-InP	MIS	BAD
V	p-Si	MIS	GOOD
V	n-InP	MIS	GOOD
VI	n-InP	MIS	GOOD
VII	p-Si	MOS	GOOD

Table 4.2 shows which deposition groups yielded good MIS or MOS capacitors.

From the C-V and I-V measurements, it was clear that of the Group III films only the non-phosphorus rich PECVD silicon nitride films deposited on p-type Si substrates produced a few working MIS devices. A typical I-V measurement of one of these devices is shown in Figures 4.1 which depicts the curve of a very good MIS capacitor. Figure 4.2 shows the C-V measurement of the same device that reveals a smooth C-V curve with pretty good accumulation and inversion regions. However, the relaxation of the surface potential toward inversion causes the device to go into deep depletion, indicating that the film is poor in quality [40].

The Group III films deposited on the n-type and p-type InP substrates yielded no working MIS capacitors. This is evident in the Figures 4.3 and 4.4 which show a typical I-V and C-V measurements of one of these devices on n-type InP. The I-V curve shows a diode effect which means that there are probably pin holes in the silicon nitride films causing the current to leak through. Although the C-V measurement resembles a good C-V curve it is not a capacitor and the curves could not be duplicated. One possible explanation for this behavior is the fact that these InP substrates belong to "Set A", which means that their ohmic contact metals were deposited after the film depositions. The insulating films could have been damaged during the formation of the ohmic contacts. In addition, since the Group III ohmic contacts were deposited by electron-beam evaporation, this could have caused charge trapping in the nitride indicated by the large negative  $V_{th}$  in the p-type Si device in Figure 4.2.



## I-V CHARACTERISTICS

SAMPLE= IA105382B4

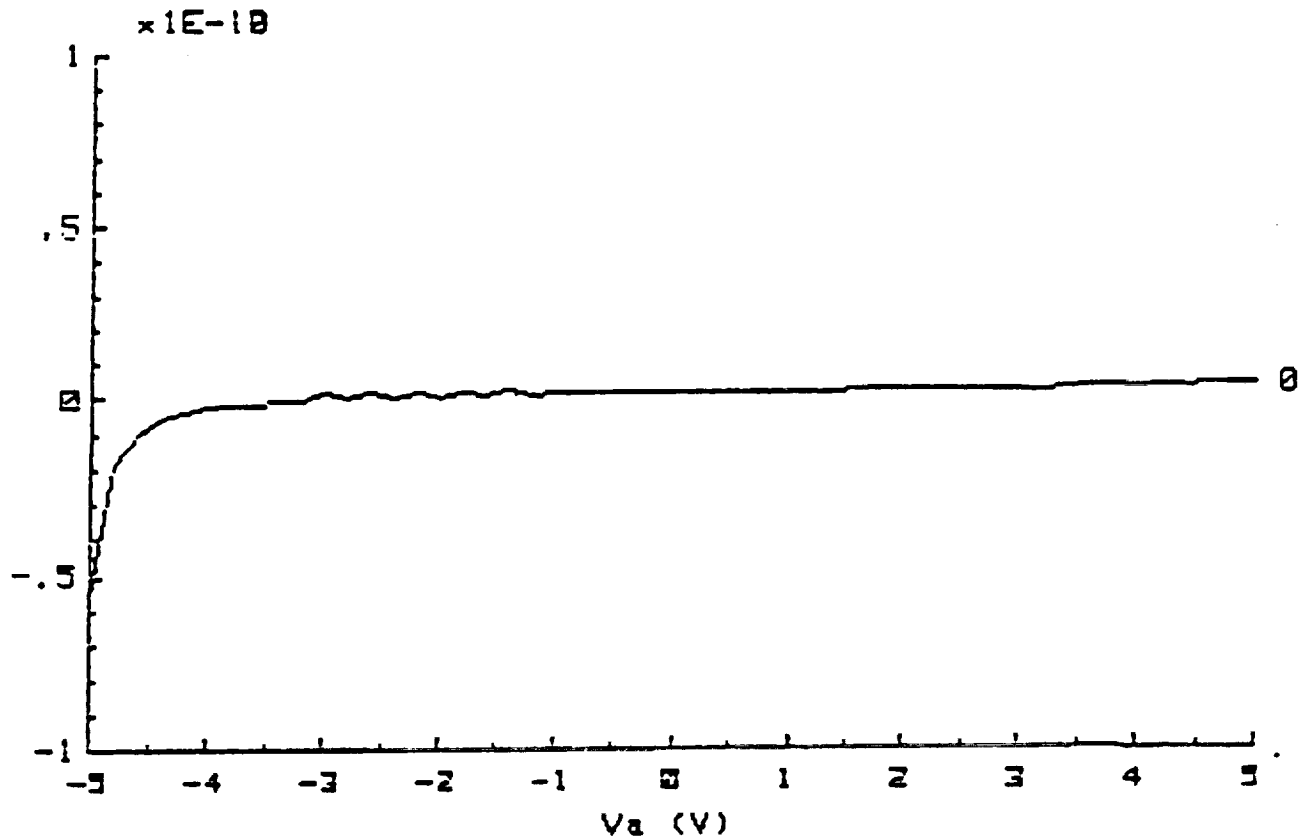


Figure 4.1 shows a typical I-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on p-type Si substrates.

## C-V CHARACTERISTICS

SAMPLE- CA10S391B4

FREQ=	1MHz	T=	298K
AREA=	$2.25E-02\text{cm}^2$	$D_{ox}$ =	500Å
$C_{ox}$ =	1524.00pF	$V_{th}$ =	-6.192V
$C_{fb}$ =	1022.91pF	$V_{fb}$ =	-7.2V
$N_{sub}$ =	$2.9E+15/\text{cm}^3$	$Q_{ss}/q$ =	$2.7E+12/\text{cm}^2$

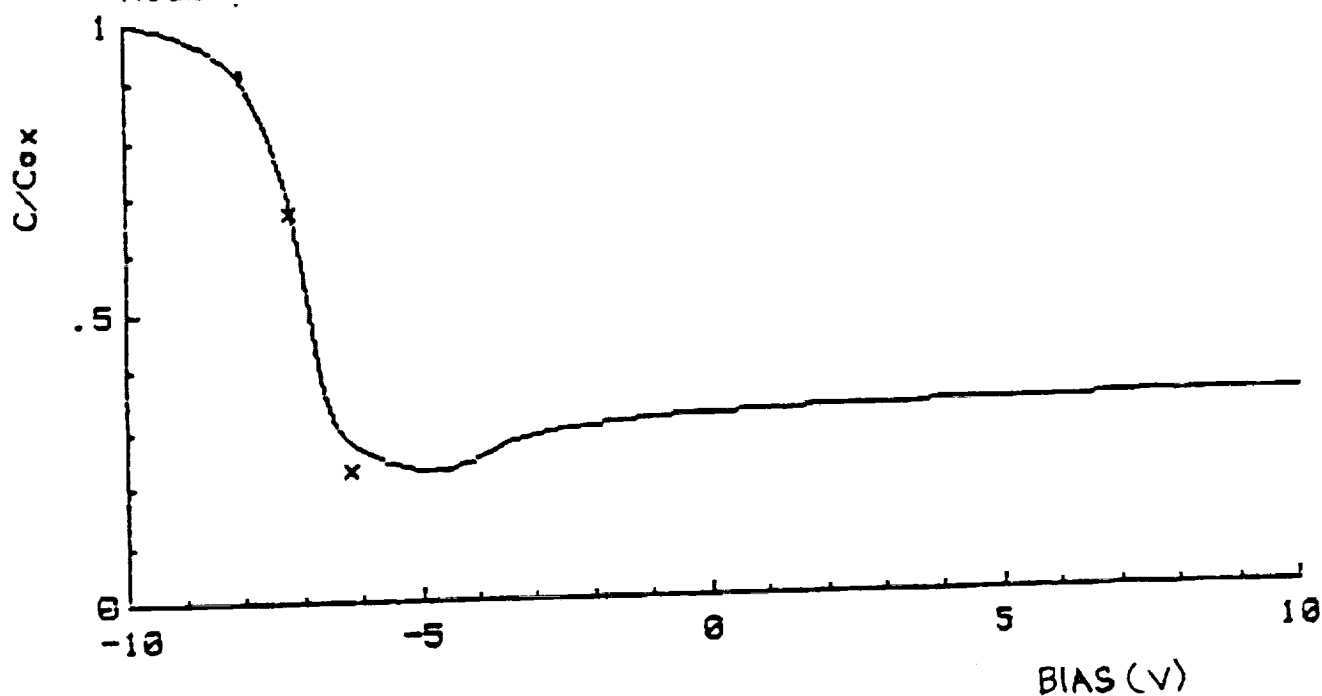


Figure 4.2 shows a typical C-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on p-type Si substrates.

## I-V CHARACTERISTICS

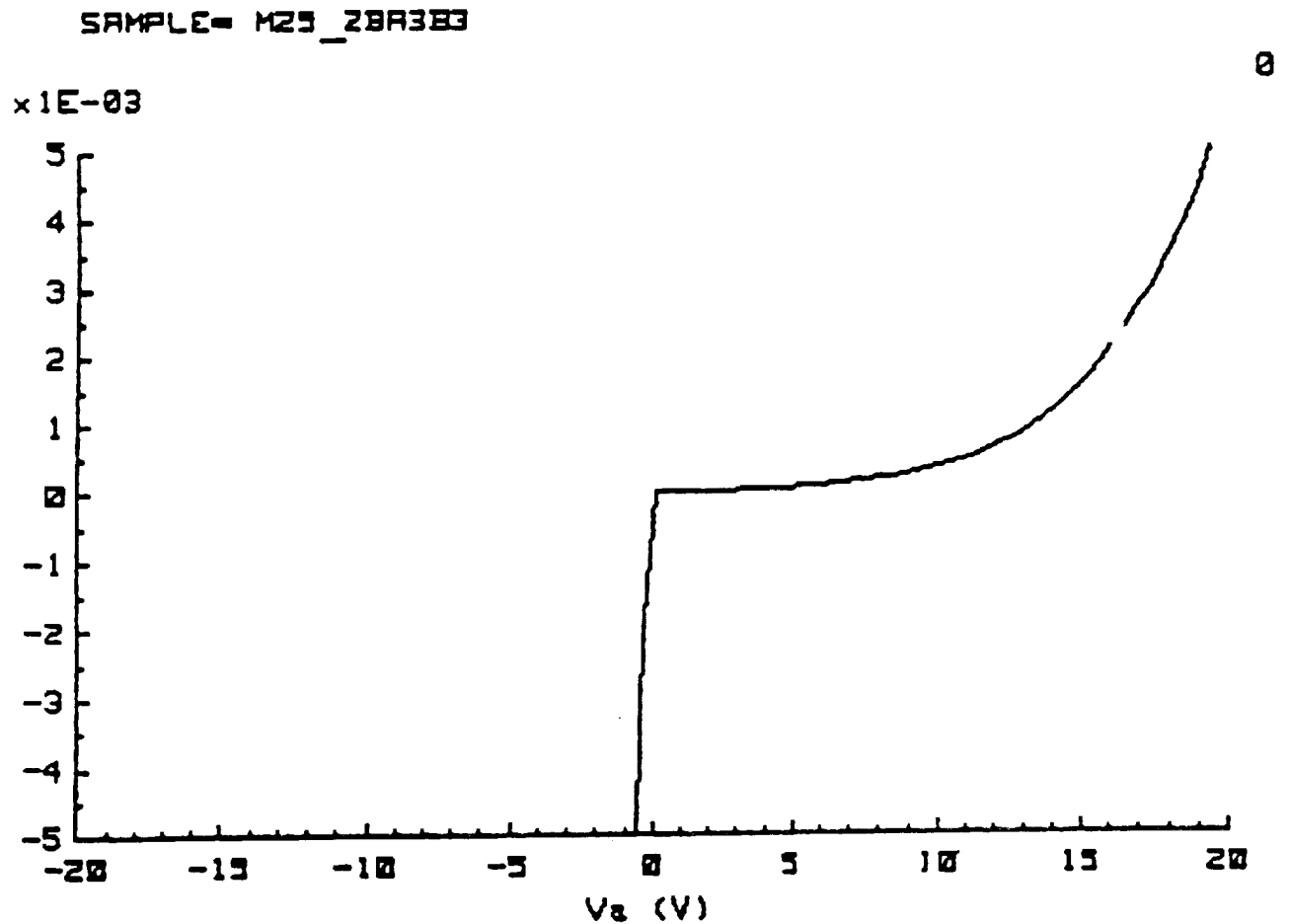


Figure 4.3 shows a typical I-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on n-type InP substrates.

## C-V CHARACTERISTICS

SAMPLE- M25\_2BA3B3

FREQ= 1MHz	T= 298K
AREA= 2.03E-01cm <sup>2</sup>	Dox= 500A
Cox= 27000.00pF	Vth= .132V
Cfb= 3732.70pF	Vfb= .6V
Nsub= 6.6E+13/cm <sup>3</sup>	Qss/q= 8.1E+11/cm <sup>2</sup>

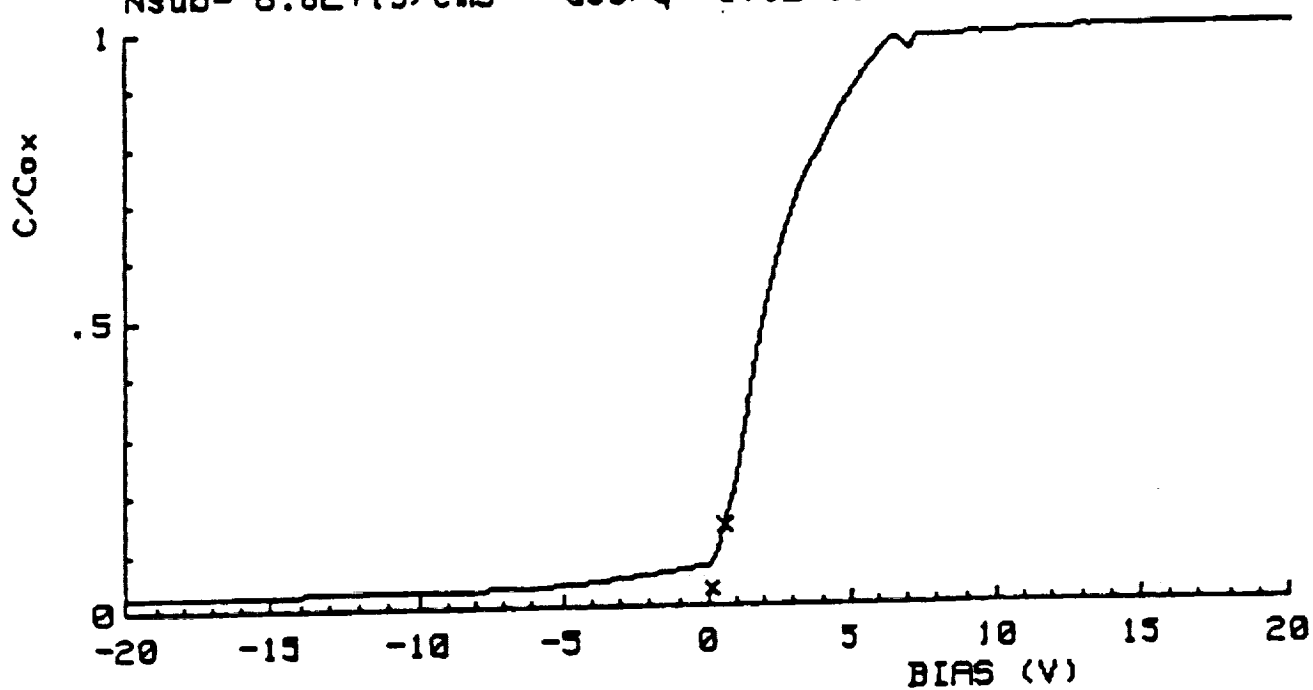


Figure 4.4 shows a typical C-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on n-type InP substrates.

A typical I-V and C-V measurement of a p-type InP device from Group III is shown in Figures 4.5 and 4.6 respectively. The I-V curve indicates the the device is not a diode but is still leaky. The C-V curve shows no clear accumulation and depletion regions. Besides the probability that the insulating film is poor, the doping concentration of these p-type substrates could be too high to invert the surface.

This same problem could be effecting the p-type InP substrates in Group V, since these were the only samples in this group that did not have any working MIS capacitors. This is again evident in the sample C-V measurement in Figure 4.7 which shows the device not quite being able to reach complete inversion. This same effect is repeated even for large increases in the positive bias limit. Figure 4.8 shows the I-V curve which resembles a diode.

Once again the p-type Si substrates in the Group V phosphorus rich PECVD silicon nitride films yielded a number of working MIS capacitors. Figure 4.9 shows a typical I-V measurement of one of these devices which appears to be have very little leakage, the sign of a good capacitor. In addition, the C-V measurement of this same device in Figure 4.10 shows a smooth C-V curve with well shaped accumulation and inversion regions. The large negative  $V_{th}$  once again indicates trapping in the nitride which may be due to the fact that the film is rich in phosphorus.

## I-V CHARACTERISTICS

SAMPLE= M30\_15A2C1

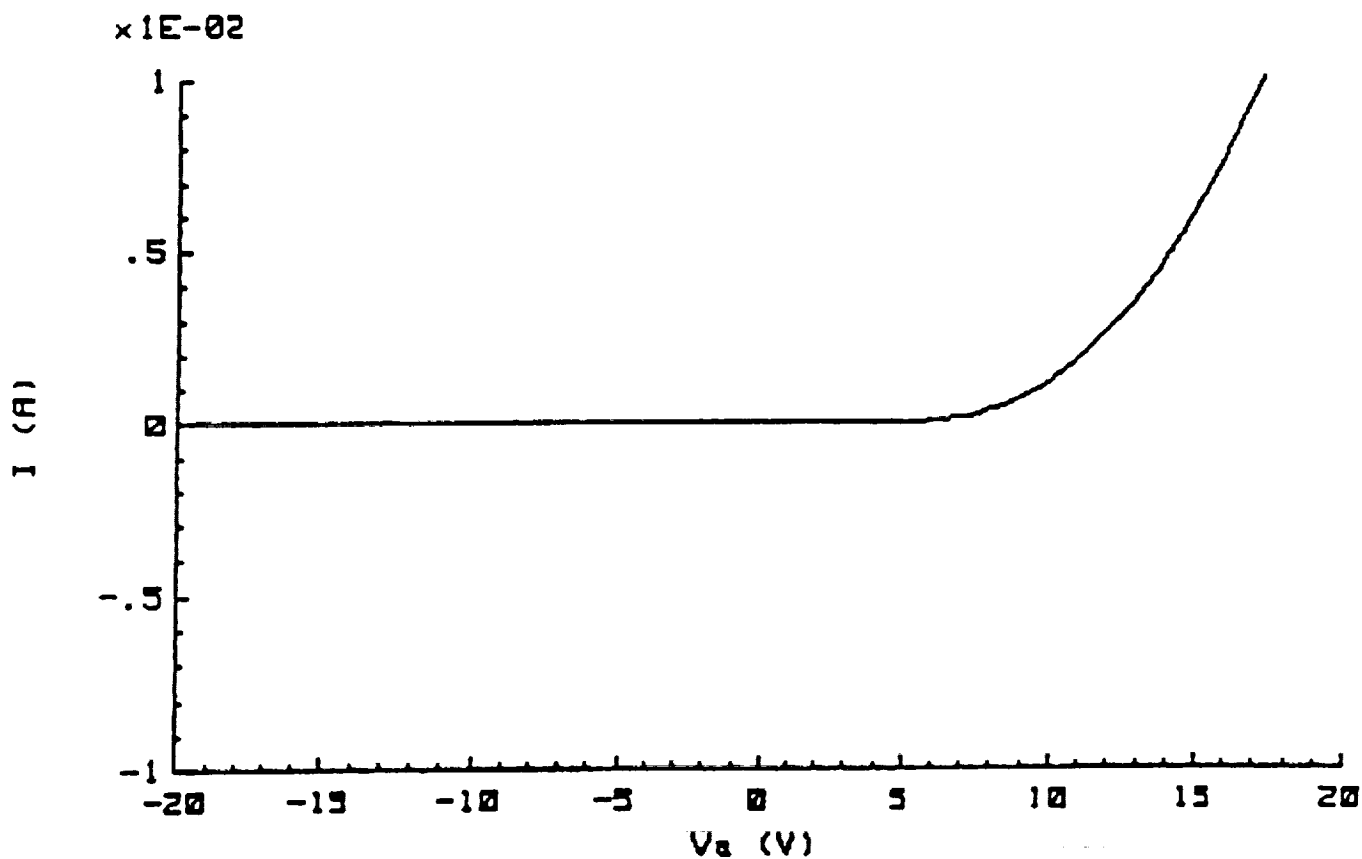


Figure 4.5 shows a typical I-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on p-type InP substrates.

## C-V CHARACTERISTICS

SAMPLE- M30\_15A2C1

FREQ=	1MHz	T=	298K
AREA=	1.31E-02cm <sup>2</sup>	Dox=	500Å
Cox=	1743.00pF	Vth=	.8953V
Cfb=	380.18pF	Vfb=	.35V
Nsub=	2.0E+14/cm <sup>3</sup>	Qss/q=	1.0E+12/cm <sup>2</sup>

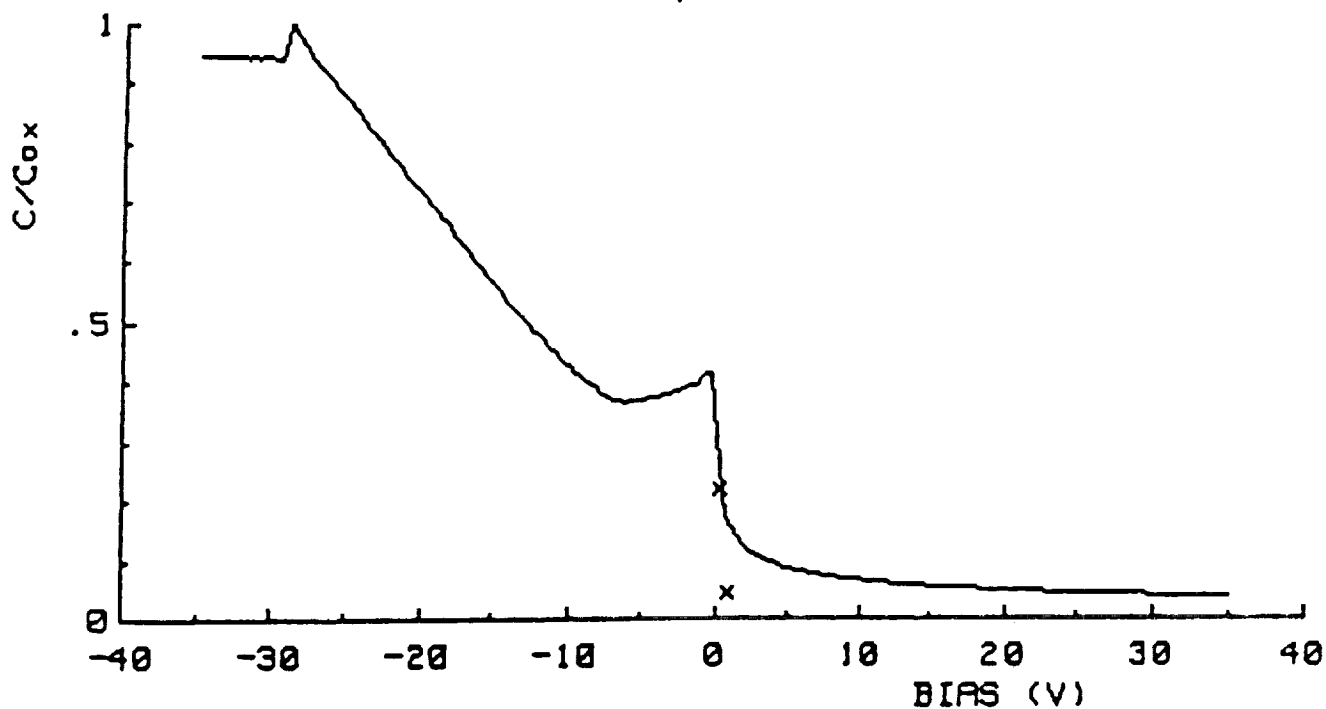


Figure 4.6 shows a typical C-V measurement for the Group III non-phosphorus rich PECVD silicon nitride films on p-type InP substrates.

## C-V CHARACTERISTICS

SAMPLE- 813\_BA1L5

FREQ= 1MHz

AREA=  $3.14E-02\text{cm}^2$

$C_{ox}$ = 1220.00pF

$C_{fb}$ = 968.00pF

$N_{sub}$ =  $3.3E+15/\text{cm}^3$

$C_{min}$ = 429.00pF

$D_{ox}$ = 1709A

$V_{th}$ = 6.342V

$V_{fb}$ = 5V

$Q_{ss}/q$ =  $1.4E+12/\text{cm}^2$

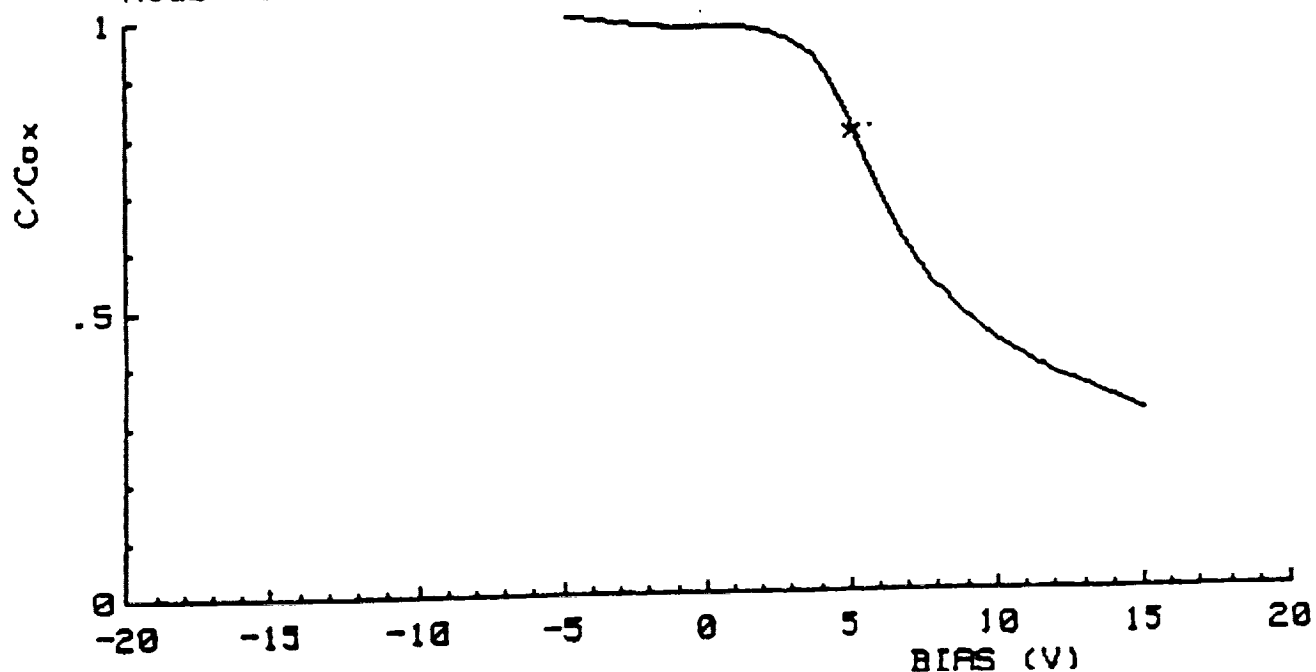


Figure 4.7 shows a typical C-V measurement for the Group V phosphorus rich PECVD silicon nitride films on p-type InP substrates.



## I-V CHARACTERISTICS

SAMPLE= 1813\_6A14.5

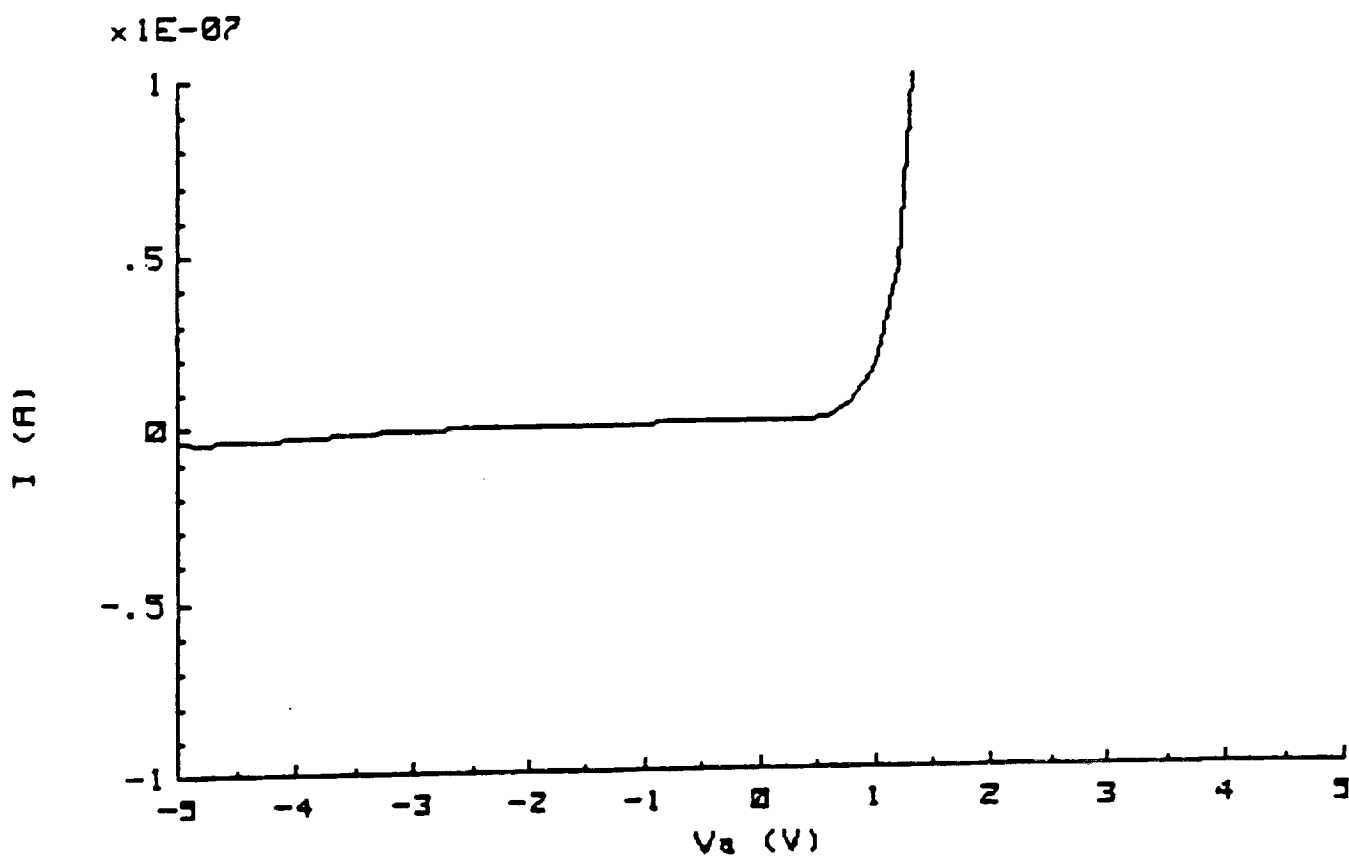


Figure 4.8 shows a typical I-V measurement for the Group V phosphorus rich PECVD silicon nitride films on p-type InP substrates.

## I-V CHARACTERISTICS

SAMPLE= 1512\_PY1A1

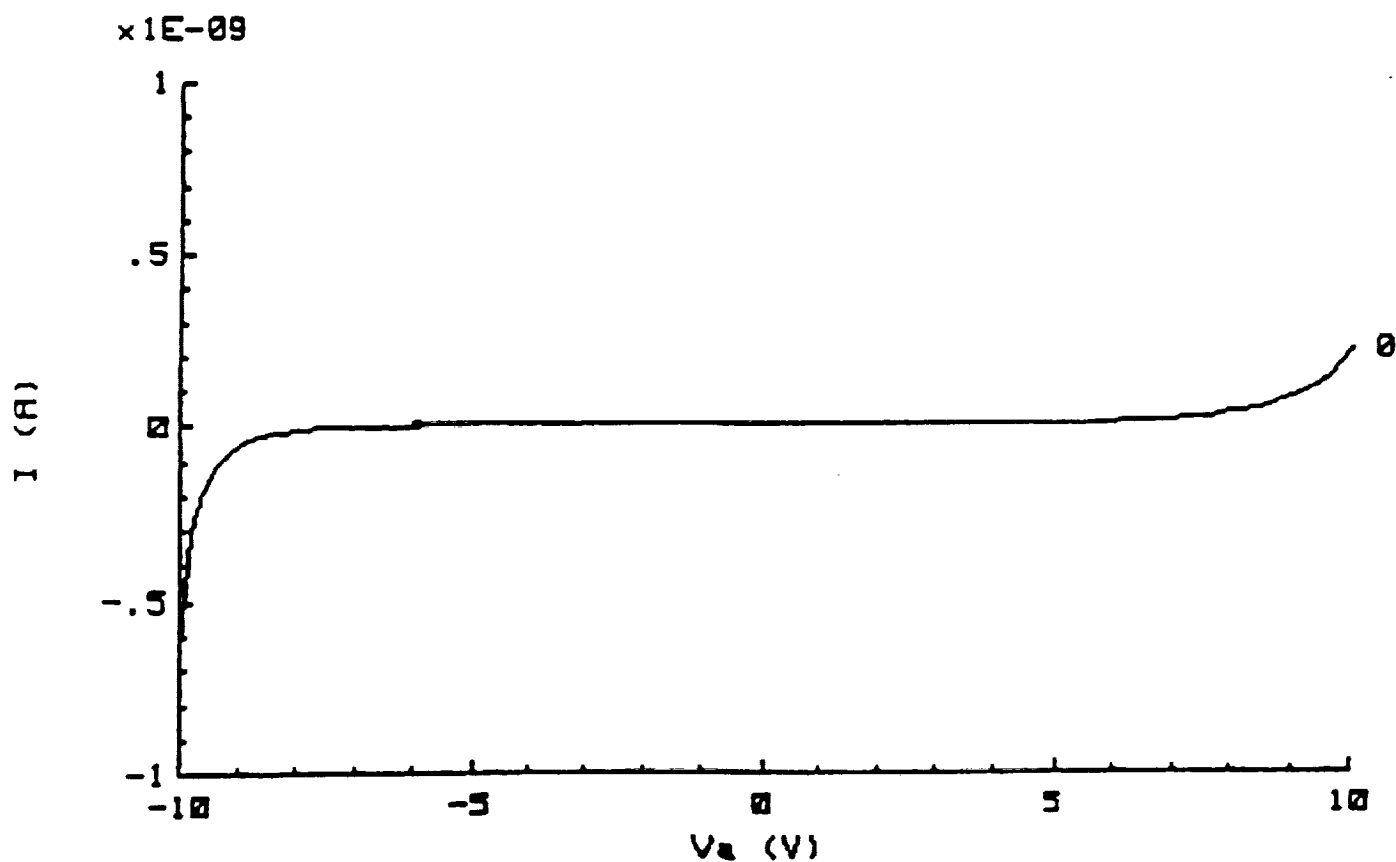


Figure 4.9 shows a typical I-V measurement for the Group V phosphorus rich PECVD silicon nitride films on p-type Si substrates.

## C-V CHARACTERISTICS

SAMPLE- CS12\_PY1A1

FREQ=	1MHz	T=	298K
AREA=	7.85E-03cm <sup>2</sup>	Dox=	329.4A
Cox=	806.00pF	Vth=	-8.913V
Cfb=	638.46pF	Vfb=	-10.4V
Nsub=	2.2E+16/cm <sup>3</sup>	Qss/q=	8.0E+12/cm <sup>2</sup>

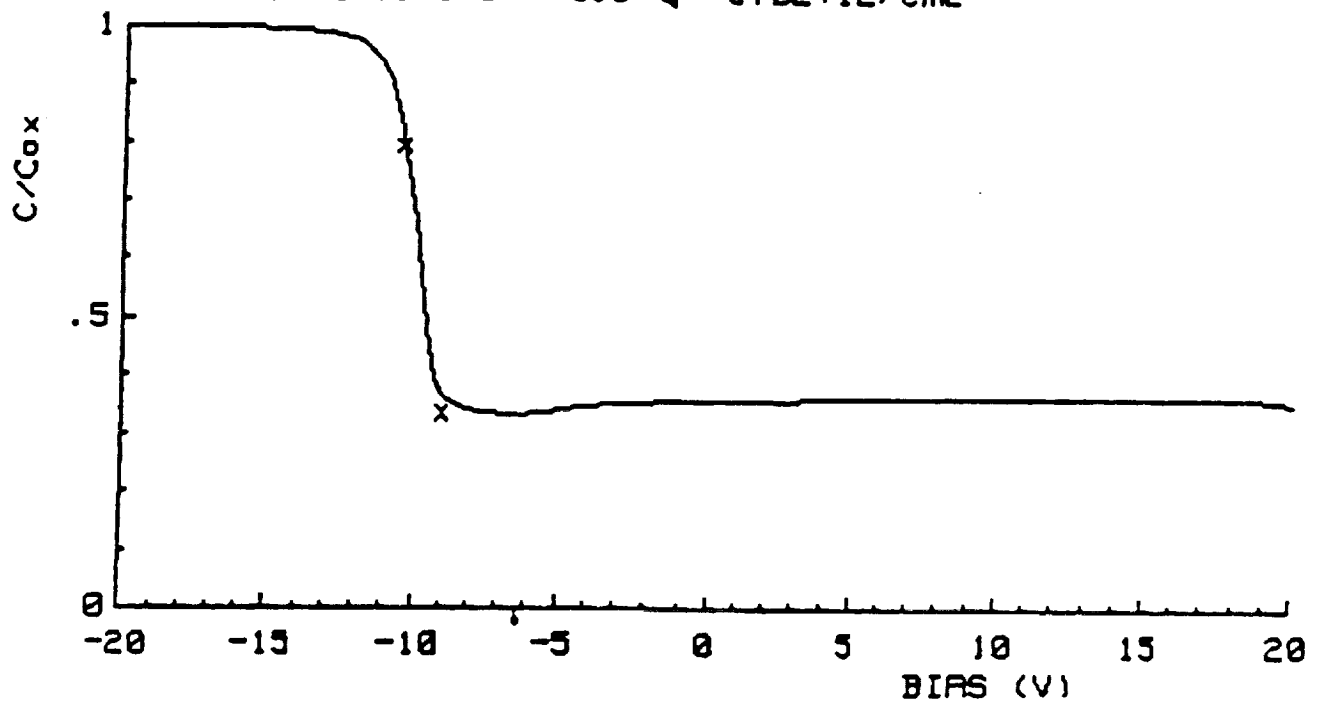


Figure 4.10 shows a typical C-V measurement for the Group V phosphorus rich PECVD silicon nitride films on p-type Si substrates.

Extraordinarily, the Group V n-type InP samples with the phosphorus rich PECVD silicon nitride films resulted in many working MIS capacitor devices. This was a major accomplishment, otherwise the electron-beam irradiation experiments to follow could not have been characterized. Figure 4.11 shows a typical C-V measurement of one of these InP MIS devices. This C-V curve is one of the few and one of the best for this kind of device. The curve is very smooth with very good accumulation and inversion regions. In addition, the I-V measurement for this device (Figure 4.12) indicates that it is a capacitor, even though it is slightly leaky.

The phosphorus rich PECVD silicon dioxide on n-InP samples in Group VI have also yielded many good MIS capacitors. This is evident from the C-V measurement of a typical device in Figure 4.13 which shows another smooth C-V curve with very well defined accumulation, depletion and inversion regions. The I-V curve in Figure 4.14 indicates little leakage as well.

Of course, the thermal silicon nitride films on p-type Si substrates in Group VII all produced very good MOS capacitors. Figure 4.15 shows a C-V measurement of a typical MOS device. The C-V curve is as expected very good. The  $V_{th}$  is a little large however, but that will not effect the experiment.

## C-V CHARACTERISTICS

SAMPLE- 721\_11B7B4

FREQ= 1MHz	Cmin= 814.00pF
AREA= 3.14E-02cm <sup>2</sup>	Dox= 729.1A
Cox= 2060.00pF	Vth= -.8642V
Cfb= 2135.34pF	Vfb= .4V
Nsub= 1.1E+15/cm <sup>3</sup>	Qss/q= 3.7E+11/cm <sup>2</sup>

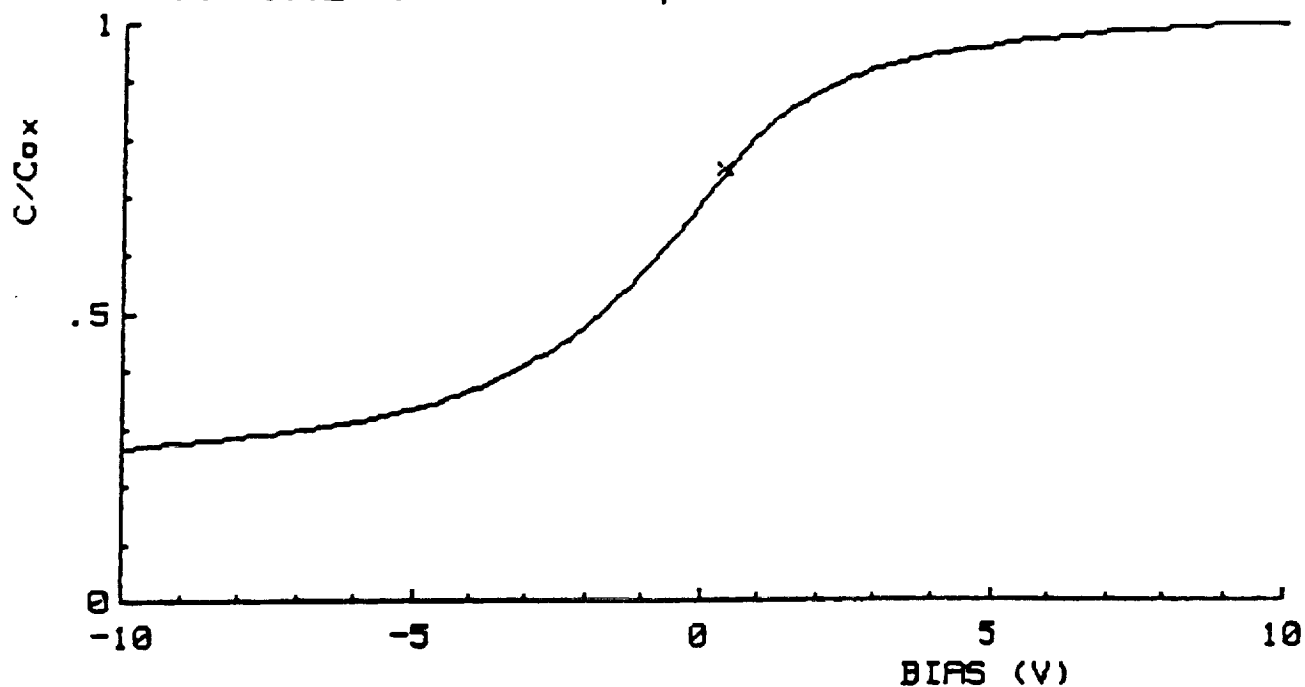


Figure 4.11 shows a typical C-V measurement for the Group V phosphorus rich PECVD silicon nitride films on n-type InP substrates.

## I-V CHARACTERISTICS

SAMPLE= I7211186B4

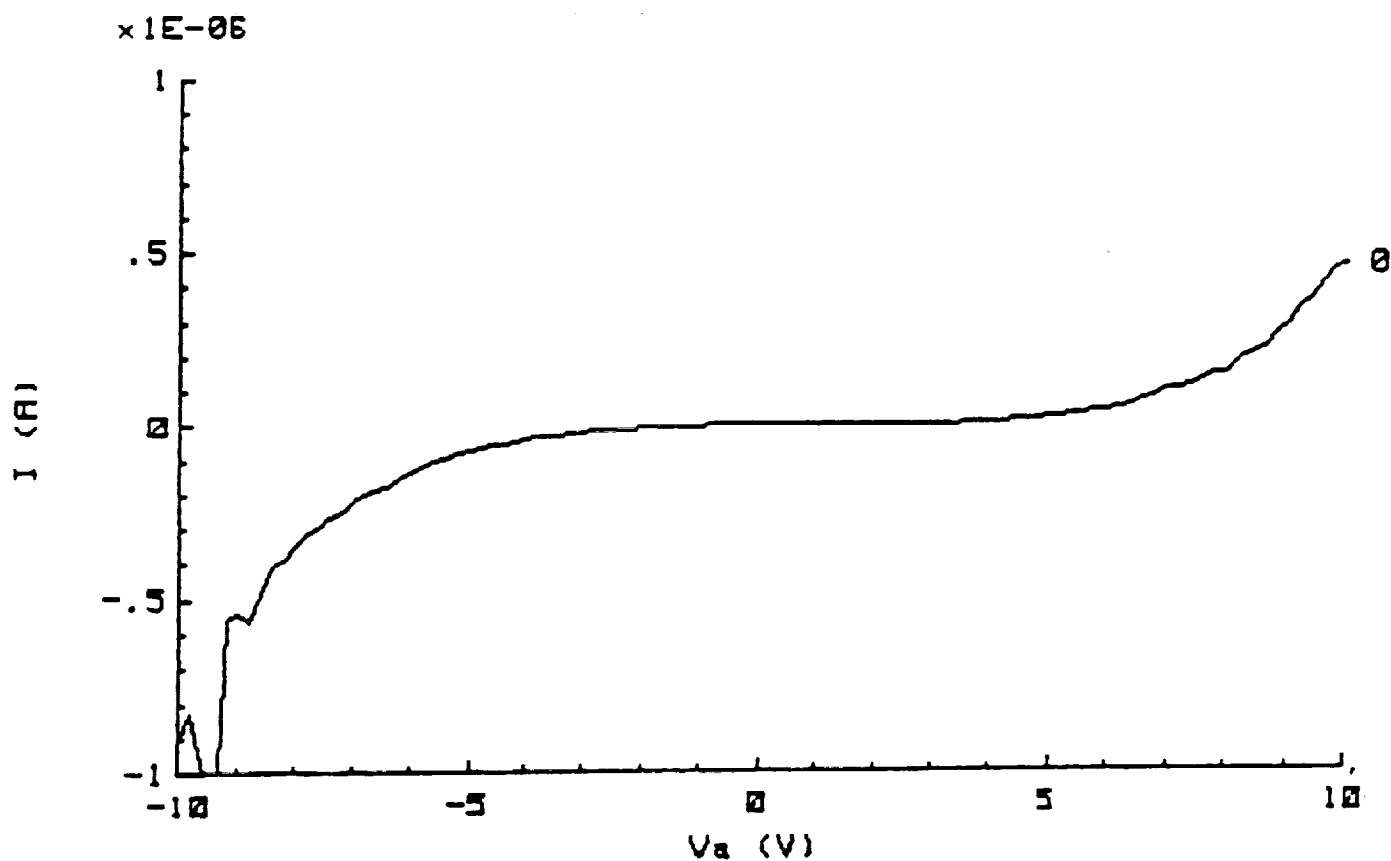


Figure 4.12 shows a typical I-V measurement for the Group V phosphorus rich PECVD silicon nitride films on n-type InP substrates.

## C-V CHARACTERISTICS

SAMPLE- 817\_1A4C4

FREQ= 1MHz	Cmin= 505.00pF
AREA= 3.14E-02cm <sup>2</sup>	Dox= 503.3A
Cox= 2110.00pF	Vth= 1.449V
Cfb= 1457.85pF	Vfb= 2.5V
Nsub= 3.3E+15/cm <sup>3</sup>	Qss/q= 1.2E+12/cm <sup>2</sup>

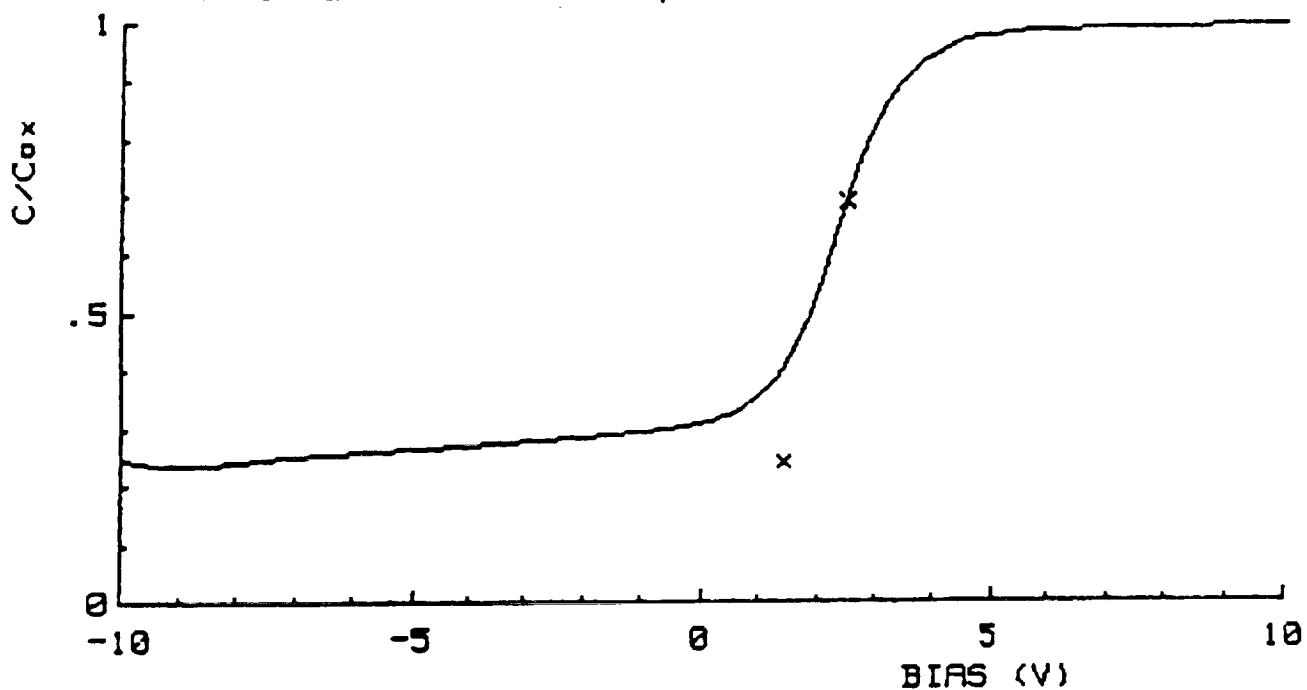


Figure 4.13 shows a typical C-V measurement for the Group VI phosphorus rich PECVD silicon dioxide films on n-type InP substrates.

## I-V CHARACTERISTICS

SAMPLE= I817\_1A1C3

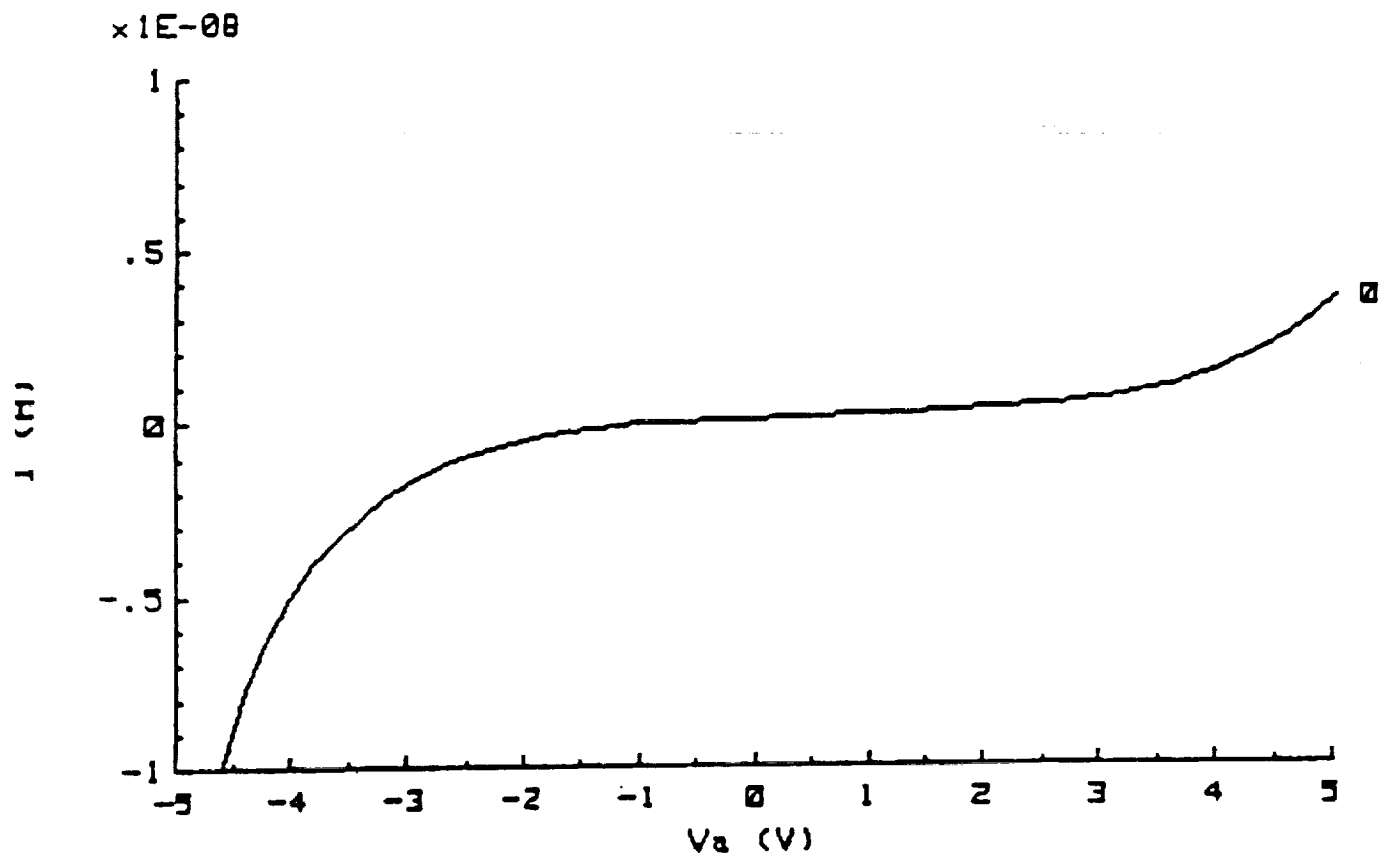


Figure 4.14 shows a typical I-V measurement for the Group VI phosphorus rich PECVD silicon dioxide films on n-type InP substrates.



## C-V CHARACTERISTICS

SAMPLE= 102\_S21B2

Freq= 1MHz

Temp= 296.9K

C<sub>min</sub>= 239pF

Area= 3.14E-02cm<sup>2</sup>

Dox= 830A

V<sub>th</sub>-V<sub>fb</sub>= 2V

C<sub>ox</sub>= 1290pF

V<sub>th</sub>= -6.91V

AQ<sub>b</sub>/C<sub>ox</sub>= -.3V

C<sub>fb</sub>= 837pF

V<sub>fb</sub>= -9.7V

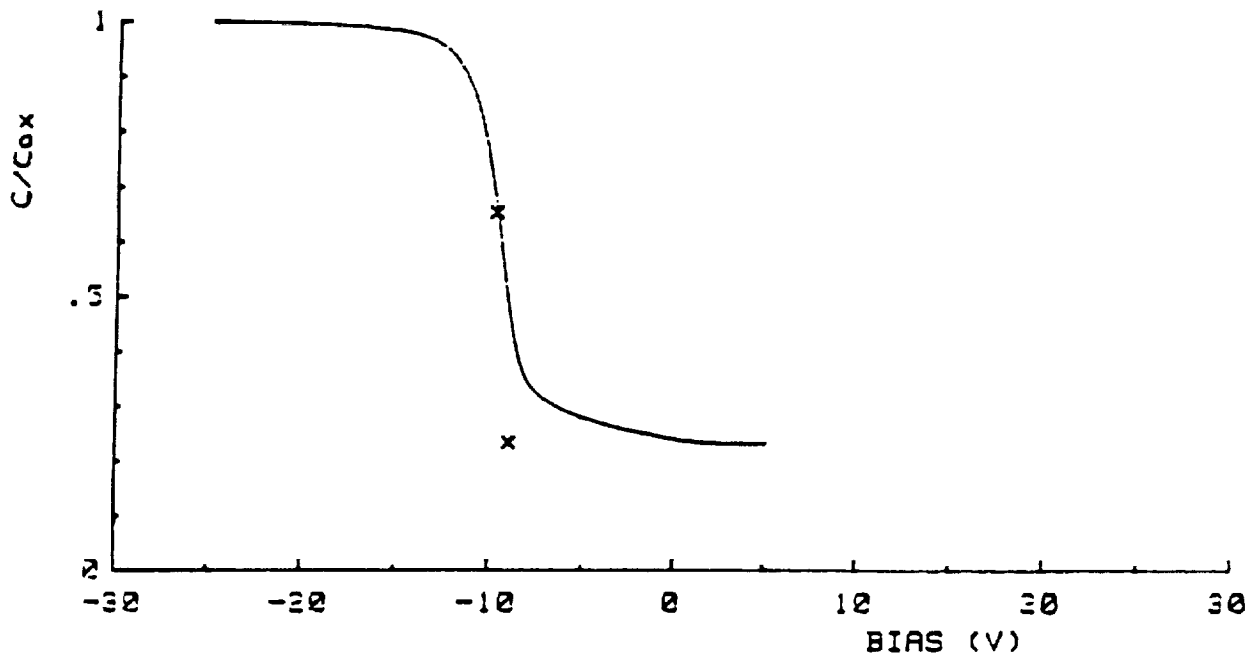


Figure 4.15 shows a typical C-V measurement for the Group VII thermal silicon dioxide films on p-type Si substrates.

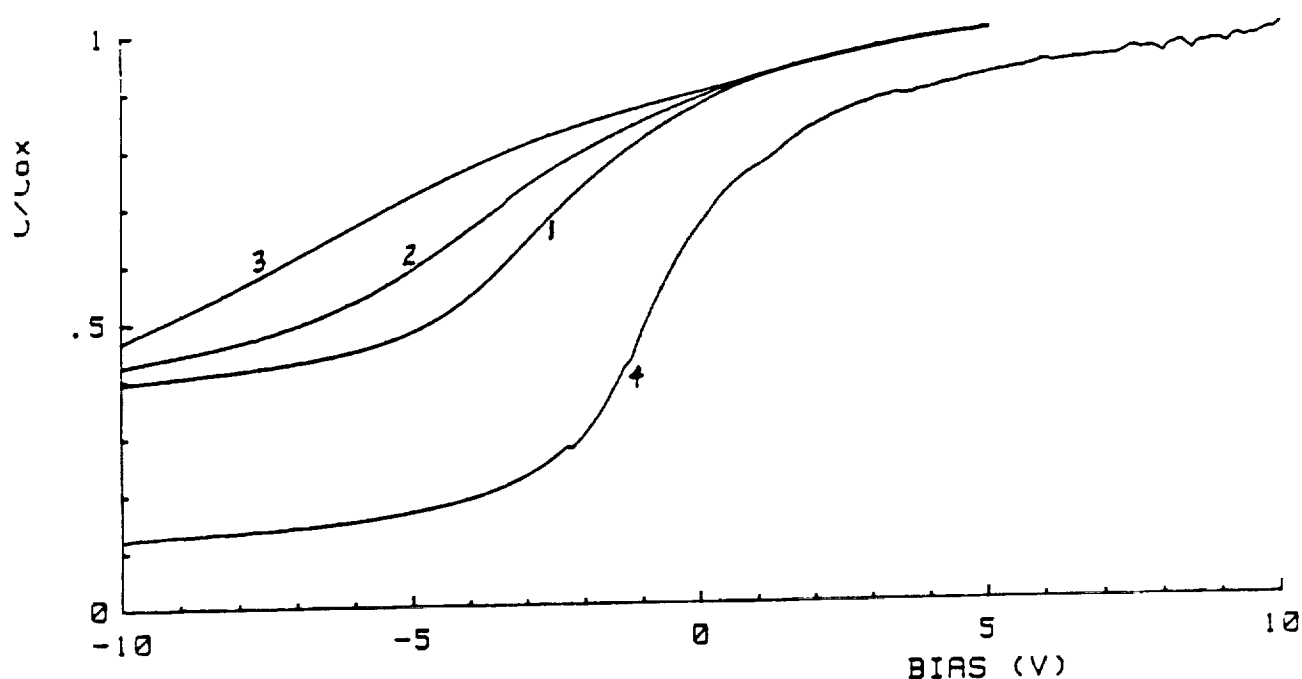
#### 4.3 ELECTRON-BEAM DAMAGE AND ANNEALING RESULTS

The electron beam irradiation of the unannealed, phosphorus rich, PECVD silicon nitride MIS capacitors from Group V seemed to cause damage to the silicon nitride-InP interface. This is evident in Figure 4.16 which shows the C-V curves before and after irradiations at 20 keV. In this figure and in the C-V curves to follow, each C-V curve represents a typical curve obtained from the set of C-V measurements, having the  $V_{th}$  and space charge voltage ( $A*Q_b/C_{ox}$ ) values near the average values for the set of measurements. Curve #1 is the initial C-V measurement, while curve #2 and #3 were taken after total exposures of  $1.0 \times 10^{-5}$  and  $1.0 \times 10^{-3}$  C/cm<sup>2</sup> respectively. The initial C-V curve shows a stretching out effect both at the accumulation and inversion regions. This stretching effect seems to increase dramatically with increasing exposure especially in the inversion region. This phenomenon can be explained by a large increase in the interface state density at the conduction and valence bands [16].

An examination of the following calculated values was obtained from the C-V measurement:  $V_{th}$ , flatband voltage ( $V_{fb}$ ), flatband capacitance ( $C_{fb}$ ), dielectric capacitance ( $C_{ox}$ ) and surface potential ( $A*Q_b/C_{ox}$ ). It was discovered that the  $A*Q_b/C_{ox}$  term remained constant during each set of 5 to 10 C-V measurements, while changing for each electron-beam exposure. Therefore this space charge voltage term of the threshold voltage was used to characterize the extent of radiation damage.

## SIN ON InP C-V CHARACTERISTICS

1. SAMPLE = INITIAL  $A*Q_b/C_{ox} = 1.45V$   
 2. SAMPLE =  $1.11E-5 C/cm^2$   $A*Q_b/C_{ox} = 1.66V$   
 3. SAMPLE =  $1.11E-3 C/cm^2$   $A*Q_b/C_{ox} = 2.01V$   
 4. SAMPLE = H<sub>2</sub>/N<sub>2</sub> ANNEAL AT 400C  $A*Q_b/C_{ox} = .283V$

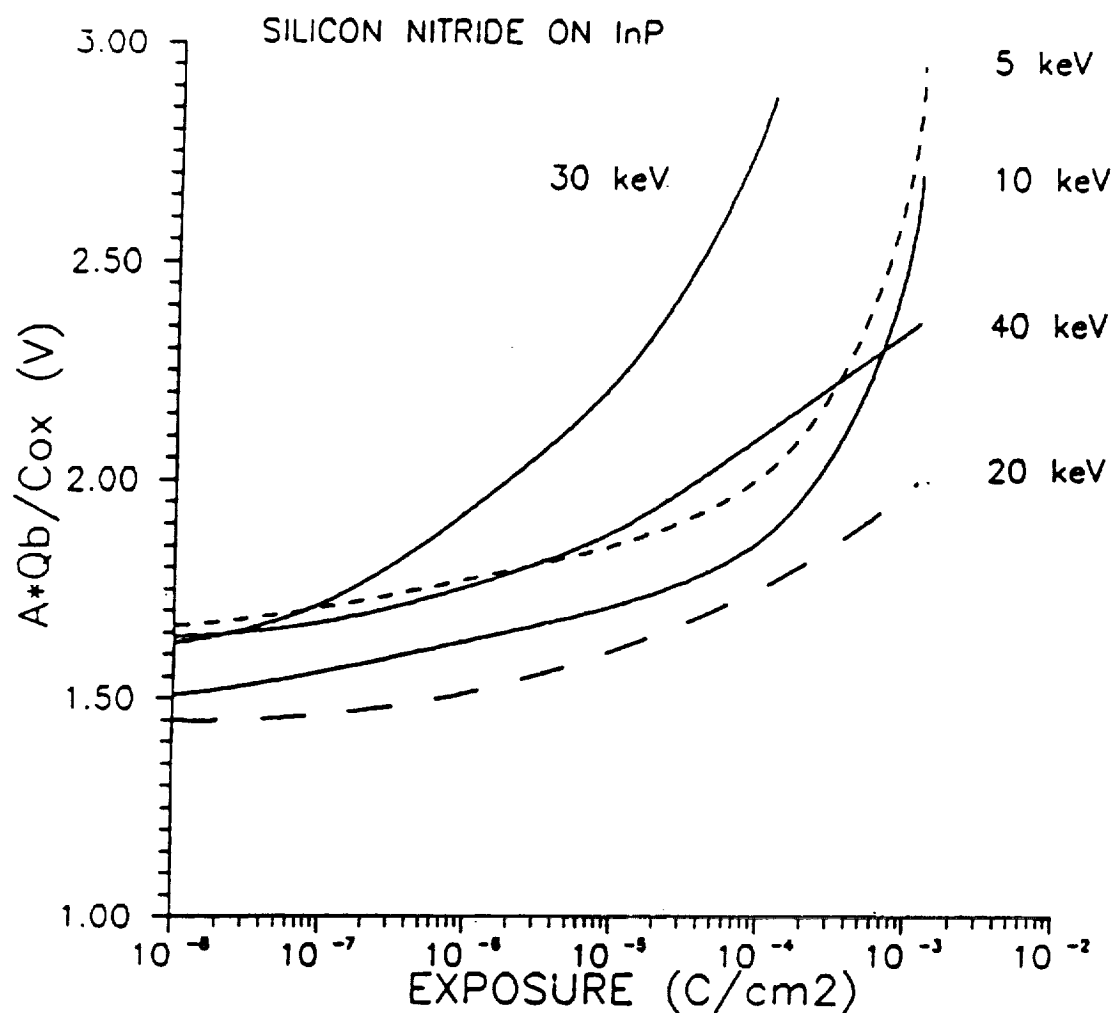


**Figure 16** C-V characteristics of the unannealed PECVD phosphorus rich interface silicon nitride on InP sample. Curve #1 is the as deposited initial measurement, while curves #2 and #3 were taken after doses of  $1.0 \times 10^{-5} C/cm^2$  and  $1.0 \times 10^{-3} C/cm^2$  respectively. Curve #4 was taken following a H<sub>2</sub>/N<sub>2</sub> anneal at 400 C for 15 min.

In curve #4 it is evident that a 5 min  $H_2/N_2$  anneal at 400 C greatly reduced the stretching of the C-V curve. This implies that there was a reduction in the interface state density. There was also a dramatic decrease in the space charge voltage term from 2.01 V after the last irradiation to .28 V after the  $H_2/N_2$  anneal. This was a shift of 1.73 V and is 1.17 V less than the original value of 1.45 V.

Similar results were found for electron-beam energies ranging from 5 to 40 keV. This trend can be seen in Figure 4.17 which shows the space charge voltage as a function of exposure for five different beam energies. For all of the energies, the C-V data showed a larger shift for higher exposures, with the 30 keV curve having a much larger effect to the irradiation than the others. This can be accounted for if the maximum energy loss of a high energy electron occurs at a depth comparable to the combined thickness of the Al gate metal and silicon nitride film [38].

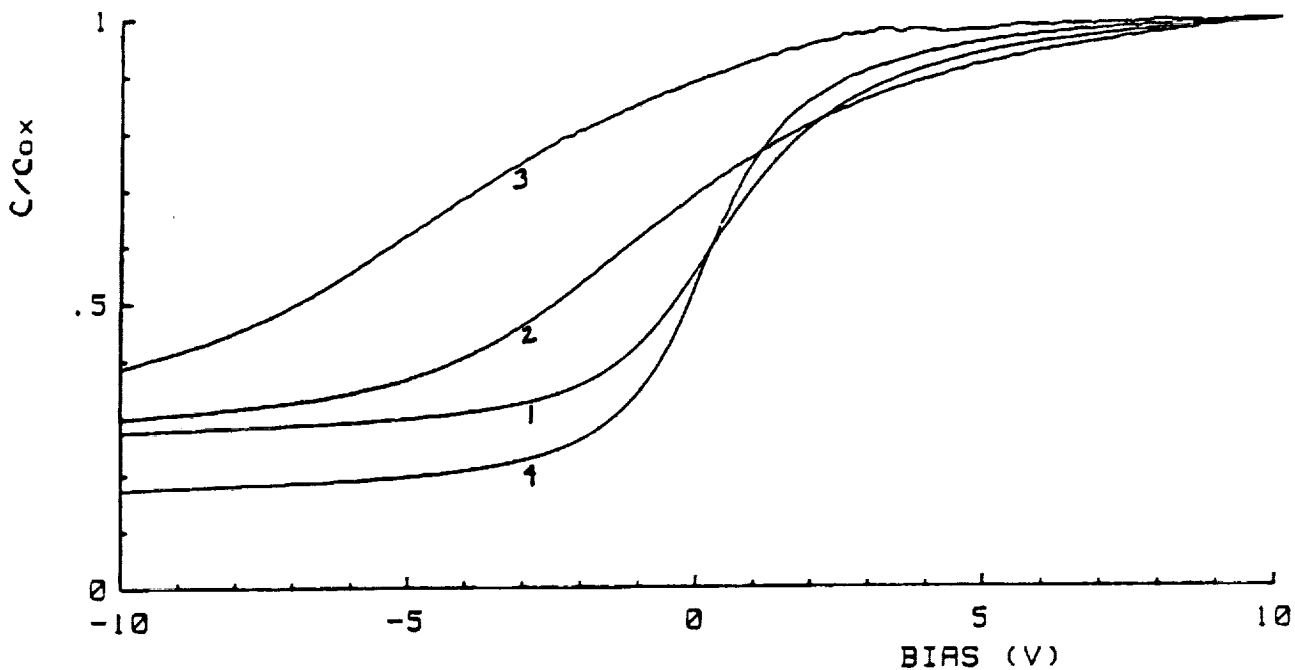
The effects of electron-beam irradiation on the C-V characteristics of the phosphorus rich PECVD silicon nitride films which were  $H_2/N_2$  annealed initially (Group VIII) are shown in Figure 4.18. Curve #1 is the C-V measurement taken immediately after the anneal. There was a slight improvement in the stretching compared to the initial curve (#1) in Figure 4.16 of the as deposited film, as well as a decrease in the space charge voltage term. However, there still was evidence of



**Figure 17** Space charge voltage vs. exposure for a range of electron beam energies of the PECVD phosphorus rich interface silicon nitride on InP sample.

## SiN ON InP C-V CHARACTERISTICS

1. SAMPLE = H<sub>2</sub>/N<sub>2</sub> ANNEAL      INITIAL  $A*Q_b/C_{ox} = .788V$   
 2. SAMPLE =  $1.11E-4C/cm^2$        $A*Q_b/C_{ox} = .887V$   
 3. SAMPLE =  $1.11E-3C/cm^2$        $A*Q_b/C_{ox} = 1.31V$   
 4. SAMPLE = H<sub>2</sub>/N<sub>2</sub> ANNEAL       $A*Q_b/C_{ox} = .439V$



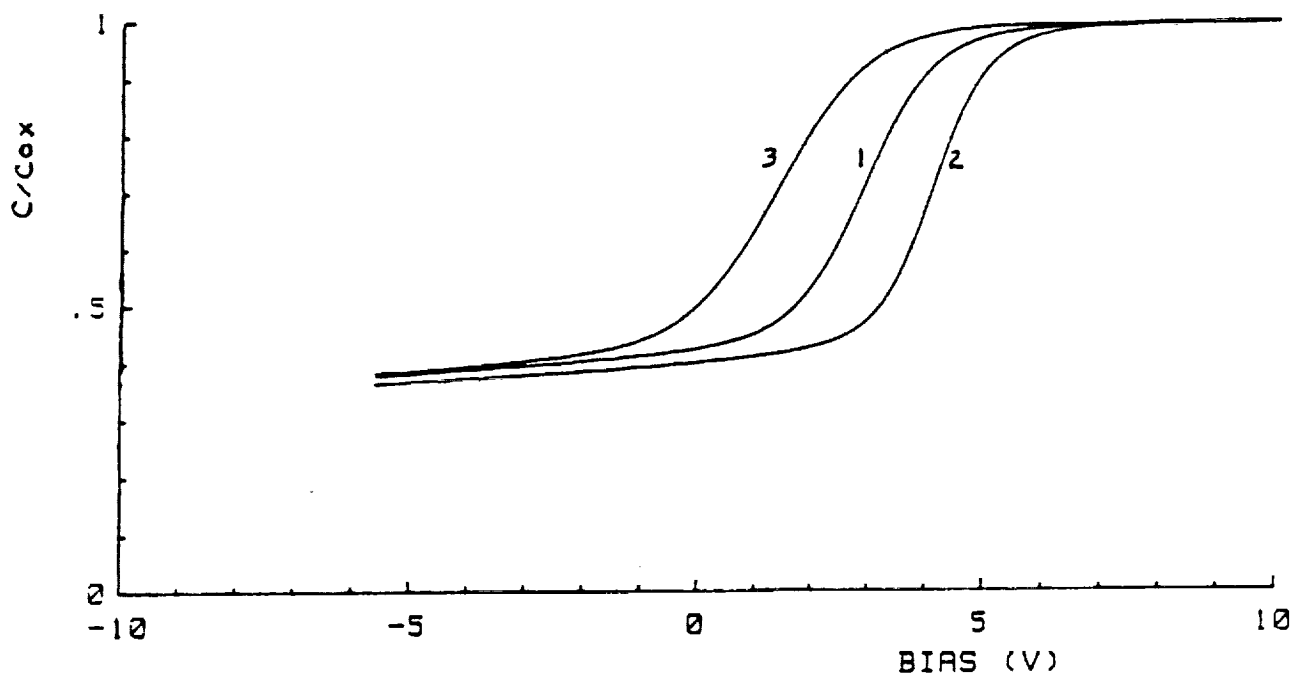
**Figure 18** C-V characteristics of the H<sub>2</sub>/N<sub>2</sub> annealed PECVD phosphorus rich interface silicon nitride on InP sample. Curve #1 was taken after the initial H<sub>2</sub>/N<sub>2</sub> anneal at 400 C for 15 min, while curves #2 and #3 were taken after doses of  $1.0 \times 10^{-4} C/cm^2$  and  $1.0 \times 10^{-3} C/cm^2$  respectively. Curve #4 was taken following the second H<sub>2</sub>/N<sub>2</sub> anneal at 400 C for 15 min after the irradiations.

interface states. There was a very large stretching out effect with increasing exposure as seen in curves #2 and #3, irradiated at 5 keV with exposures of  $1.0 \times 10^{-4}$  C/cm<sup>2</sup> and  $1.0 \times 10^{-3}$  C/cm<sup>2</sup> respectively. This sample also showed an increase in  $A^*Q_b/C_{ox}$  with increasing exposure. As before, curve #4 showed a large reduction in stretching after an H<sub>2</sub>/N<sub>2</sub> anneal, that even surpassed curve #1 after the initial H<sub>2</sub>/N<sub>2</sub> anneal. This means that the H<sub>2</sub>/N<sub>2</sub> anneal reduced the interface state density induced by the irradiation. In addition the space charge voltage which was initially .79 V was reduced from 1.31 V after the last irradiation to .44 V after the final anneal. The electron-beam exposure caused a positive shift of .52 V while the H<sub>2</sub>/N<sub>2</sub> anneal caused a negative shift of .87 V, which is .35 V less than the initial value.

The irradiation performed on the phosphorus rich PECVD silicon dioxide capacitors from Group VI is shown in Figure 4.19 for a beam energy of 20 keV. In this figure, curve #1 represents the initial C-V measurement of the as deposited silicon dioxide film. Curves #2 and #3 represent irradiations of  $1.0 \times 10^{-6}$  C/cm<sup>2</sup> and  $1.0 \times 10^{-3}$  C/cm<sup>2</sup> respectively. A strange effect occurred at the smaller exposures in curve #2. There was an almost parallel positive shift in the C-V curve. This would imply that there was negative trapped charge in the bulk of the oxide without any increase in the interface state density. However as the exposure increased in curve #3, there was a large shift in the negative direction accompanied by some stretching out of the curve in the

## SiO<sub>2</sub> ON InP C-V CHARACTERISTICS

- 1. SAMPLE= INITIAL  $A*Q_b/C_{ox}=1.25V$
- 2. SAMPLE=  $1.10E-6C/cm^2$   $A*Q_b/C_{ox}=1.16V$
- 3. SAMPLE=  $1.10E-3C/cm^2$   $A*Q_b/C_{ox}=1.28V$

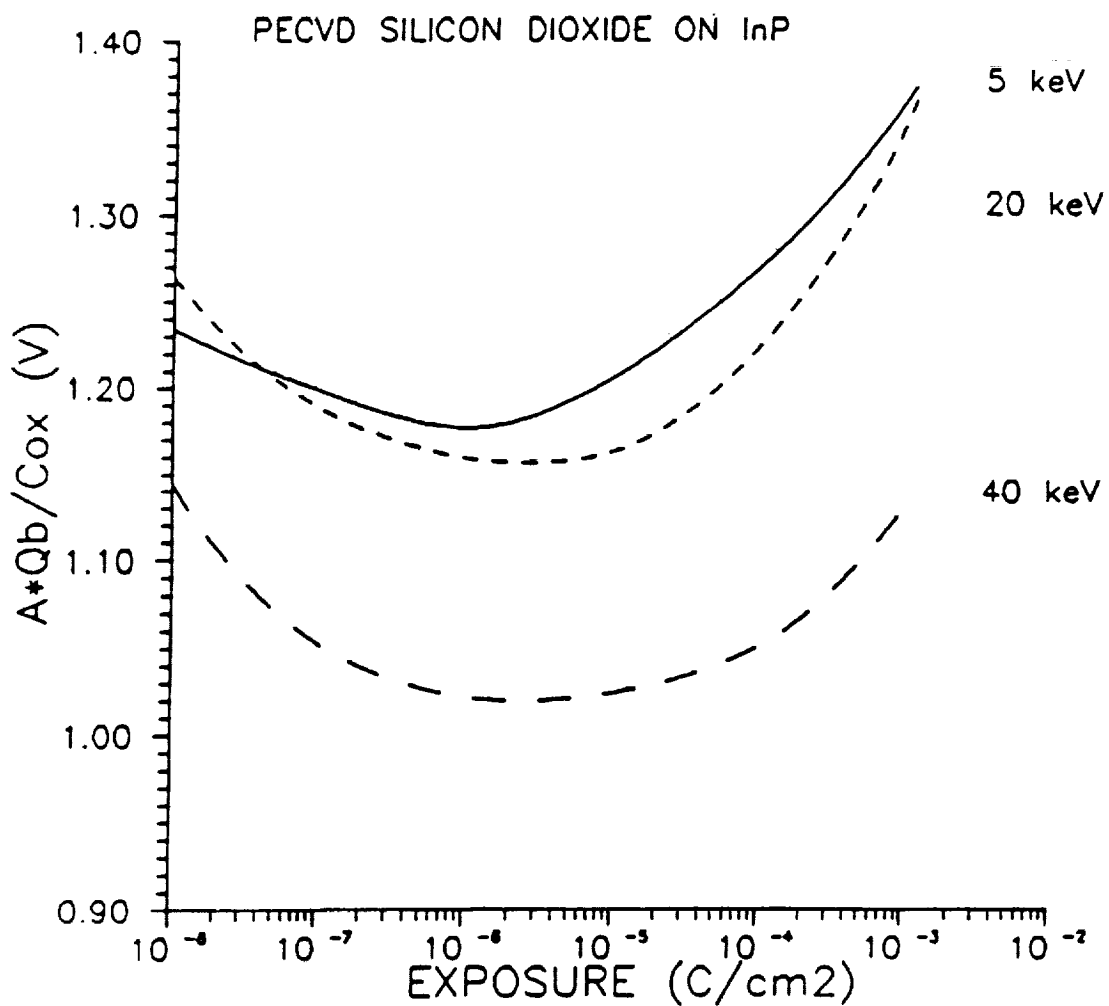


**Figure 19** C-V characteristics of the unannealed PECVD phosphorus rich interface silicon dioxide on InP sample. Curve #1 is the as deposited initial measurement, while curves #2 and #3 were taken after doses of  $1.0 \times 10^{-6} C/cm^2$  and  $1.0 \times 10^{-3} C/cm^2$  respectively.



inversion region. This implies that there was an increase in donor-like interface states near the conduction band as well as positive charge trapping or negative charge detrapping from the smaller exposures. This trend was also seen for beam energies of 5 keV and 40 keV (Figure 4.20), which shows  $A*Q_b/C_{ox}$  as a function of exposure.

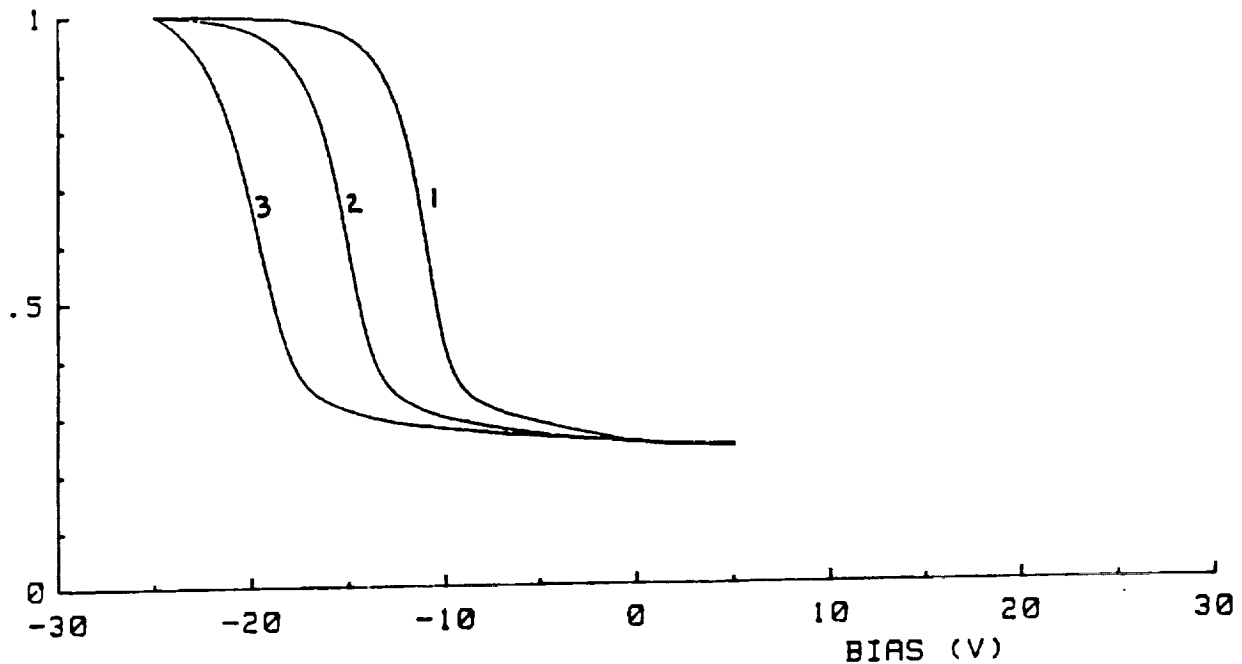
Finally, irradiations were performed on thermal silicon dioxide MOS capacitors from Group VII for comparison. These results are shown in Figure 4.21 which shows C-V curves for a range of doses at 20 keV. The initial C-V measurement is curve #1 and the C-V measurements after irradiations at exposures of  $1.0 \times 10^{-6}$  C/cm<sup>2</sup> and  $1.0 \times 10^{-3}$  C/cm<sup>2</sup> are represented by curves #2 and #3 respectively. There was an increasing negative parallel shift in the C-V curves with increasing exposure. This could have been due to a build up of positive trapped charge in the oxide bulk from the irradiation. There did not seem to be any stretching, therefore the interface state density in this sample was insignificant. Similarly, the space charge voltage was not effected by irradiation at any energy as shown in Figure 4.22. However, there was a very large shift in  $V_{th}$  due to irradiation as shown in Figure 4.23, which is valid due to the absence of interface states. This shift is on the order of 8.0 V.



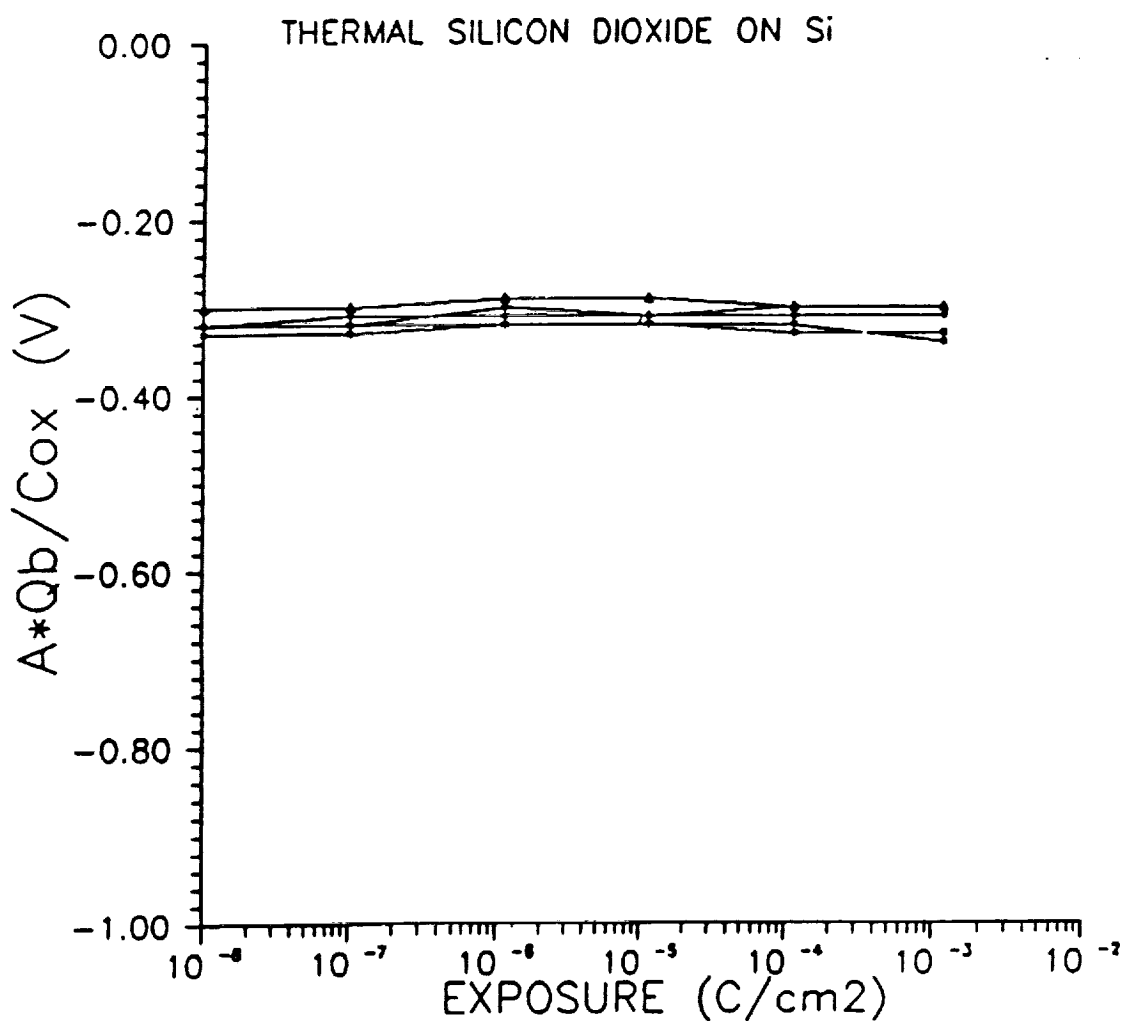
**Figure 20** Space charge voltage vs. exposure for a range of electron beam energies of the PECVD phosphorus rich interface silicon dioxide on InP sample.

## SiO<sub>2</sub> ON Si C-V CHARACTERISTICS

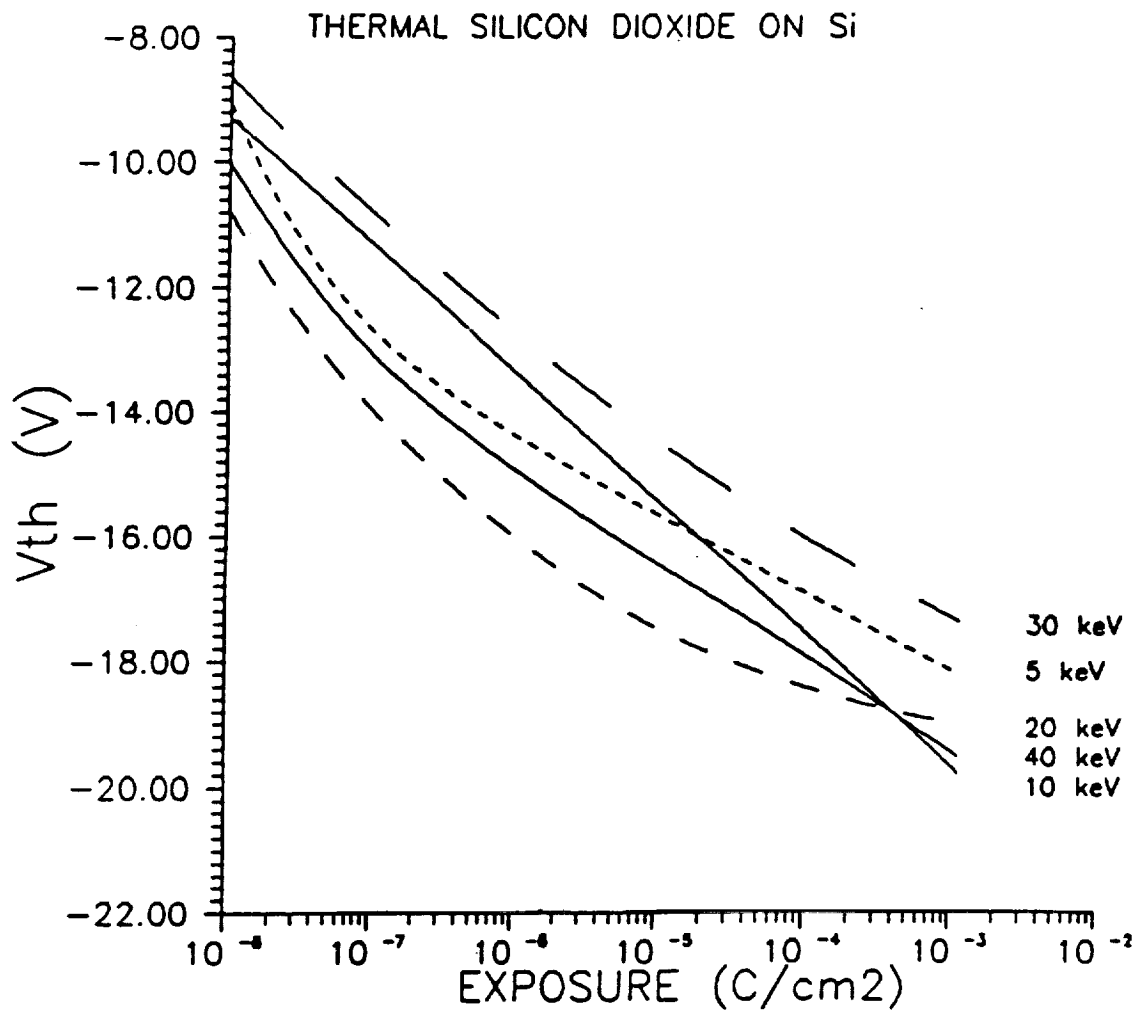
1. SAMPLE= INITIAL  $A*Q_b/C_{ox} = -.320V$   $V_{th} = -10.8V$   
 2. SAMPLE=  $1.10E-6C/cm^2$   $A*Q_b/C_{ox} = -.314V$   $V_{th} = -14.6V$   
 3. SAMPLE=  $1.11E-3C/cm^2$   $A*Q_b/C_{ox} = -.306V$   $V_{th} = -19.0V$



**Figure 21** C-V characteristics of the thermally grown silicon dioxide on Si sample. Curve #1 is the as grown initial measurement, while curves #2 and #3 were taken after doses of  $1.0 \times 10^{-6} C/cm^2$  and  $1.0 \times 10^{-3} C/cm^2$  respectively.



**Figure 22** Space charge voltage vs. exposure for a range of electron beam energies of the themally grown silicon dioxide on Si sample.



**Figure 23** Threshold voltage vs. exposure for a range of electron beam energies of the thermally grown silicon dioxide on Si sample.

## CHAPTER 5. SUMMARY

### 5.1 CONCLUSION

PECVD silicon nitride and PECVD silicon dioxide films, each with a phosphorus rich layer at the insulator/semiconductor interface, were successfully deposited on n-type InP substrates in a capacitively coupled parallel plate reactor modified for 13.56 MHz operation. The silicon nitride films were deposited using silane ( $\text{SiH}_4$ ), ammonia ( $\text{NH}_3$ ) and nitrogen ( $\text{N}_2$ ) as reactant gases. While the silicon dioxide films were deposited using  $\text{SiH}_4$  and nitrous oxide ( $\text{N}_2\text{O}$ ) as reactant gases. In addition, a dry thermally grown silicon dioxide sample on p-type silicon was used for comparison.

The thickness and refractive index of the deposited films were determined by ellipsometry. The silicon nitride films were typically deposited to a thickness of 900 Å, while the refractive index was determined to be 1.99, very close to the accepted value. In addition, all of the silicon nitride films were very uniform, with only a 10 to 20 Å difference in the film thickness between the center and the edge of the wafer. The PECVD silicon dioxide films were approximately 1500 Å thick, with an index of refraction of 1.48. While the thermal silicon dioxide film was 850 Å thick and a refractive index of 1.42. However the silicon dioxide films were not as uniform as the silicon nitride films.

The refractive index for both silicon dioxide films was close to the accepted value for silicon dioxide.

The electrical properties of the films was determined by taking current-voltage (I-V) and high frequency (1 MHz) capacitance-voltage (C-V) measurements of MIS and MOS capacitors fabricated from the films. From these measurements it was clear that only the insulating films deposited on n-type InP substrates resulted in working capacitors and only from samples in Groups V and VI.

The purpose of this study was to determine the extent of electron-beam induced damage in thin insulating films on a compound semiconductor as a function of exposure time to high energy electron beams. Electron-beam irradiation effects were investigated on phosphorus rich PECVD silicon nitride and phosphorus rich PECVD silicon dioxide on InP as well as thermal silicon dioxide on Si capacitors. From these experiments several conclusions were drawn. First of all, the electron-beam irradiation had an effect on the phosphorus rich silicon nitride capacitors, however the damage was successfully annealed and also improved the device characteristics. In fact the space charge voltage term which was initially at 1.45 V decreased from 2.01 V after the last irradiation to .28 V following the H<sub>2</sub>/N<sub>2</sub> anneal. The least radiation damage was found in the phosphorus rich silicon dioxide on InP capacitors which appeared to show little increase in the interface state density. While the most

radiation damage was caused in the thermal silicon dioxide MOS capacitors fabricated on Si which showed  $V_{th}$  shifts on the order of 8.0 V.

## 5.2 FUTURE CONSIDERATIONS

In order to get a better understanding of the electron-beam induced damage of thin insulating films on compound semiconductors, interface state density measurements have to be made before and after irradiations, as well as after annealing experiments. In addition a more in depth study of annealing effects after irradiations must be made. Including a long range study of irradiations followed by annealing and irradiations again. This procedure would determine whether the post radiation anneals are actually healing the damaged films.



## REFERENCES

1. R. Singh, "Thin Gate Dielectrics For Si and InP IC's", Proceedings of ECS, Vol-87-10, 1986, ed (V. J. Kapoor and K. T. Hankins)
2. D. Howard Phillips, "Submicron Lithography Radiation Damage in Silicon and GaAs IC's" Proc. of SPIE, Vol 393 14-15 March 83 (E-Beam, X-Ray and Ion Beam Technique for Submicron Lithographies II, p. 70)
3. J. M. Aitken, D. R. Young, K. Pan, "Electron Trapping in Electron-Beam Irradiated SiO<sub>2</sub>" J. Appl. Phys, 49(6), June 1978, p. 3386-3391
4. J. M. Aitken, "lum MOSFET VLSI Technology: Part VIII - Radiation Effects", IEEE Transactions on Electron Devices, Vol ed 26, No. 4, April, 1979
5. T. Kato, Y. Watakabe, K. Saitoh, M. Morimoto, "Technologies for Electron Beam Direct Writing", Microelectronic Engineering 1 (1983), 69-90, North Holland
6. H. J. Leamy, "Charge Collection Scanning Electron Microscope", J. Appl. Phys 53(6), June, 1982
7. S. Krawczyk, M. Garrigues, T. Mrabeut, "Effect of Annealing Charge Injection and Electron Beam Irradiation on the Si-SiO<sub>2</sub> Interface Barrier Heights and on the Work Function Difference in MOS Structures", 0094-243x/84/1220039-06 \$3.00 Copyright 1984 American Institute of Physics
8. B. S. H. Royce, "Radiation Induced Charge Storage in Metal-Oxide-Semiconductor Devices", International Symposium of Electrics and Dielectrics, 1975
9. M. Peckerar, R. Fulton, P. Blaise, "Radiation Effects on MOS Devices Caused by X-Ray and E-Beam Lithography", J. Vac. Sci, Technol., 16(6), Nov/Dec (1979)
10. T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schusler and H. N. Yu, "lum MOSFET VLSI Technology: Part IV - Hot Electron Design Constraints", IEEE Transactions on Electron Devices, Vol ed 26, No. 4, p 226-238, 1969
11. P. M. Lenahau and P. V. Dressendorfer, "An Electron Spin Resonance Study of Radiation Induced Electrically Active Paramagnetic Centers at the Si/SiO<sub>2</sub> Interface", J. Appl. Phys 54(3), p 1457 (1983)
12. K. H. Zaininger, IEEE Trans. Nucl. Sci., NS-13, 237 (1966)

13. P. M. Lenahan, K. L. Brower, P. V. Dressendorfer, W. J. Johnson, IEEE Trans., Nucl. Sci., NS-28, 4105, (1981)
14. T. P. Ma, G. Scoggan and R. Leone, "Comparison of Interface-State Generation by 15keV Electron Beam Irradiation in p-type and n-type MOS Capacitors", Appl. Phys. Lett., Vol 27, No. 2, 15, July, 1975
15. E. Arnold, G. Abowitz, Appl. Phys. Lett. 9, 344 (1966)
16. A. Goetzburger, E. Klausmann, M. J. Schulz, "Interface States on Semiconductor Insulation Surfaces", CRC Critical Reviews in Solid State Sciences, Jan, 1976
17. P. M. Levahan, K. L. Brower, P. V. Dressendorfer and W. C. Johnson, "Radiation Induced Trivalent Silicon Defect Buildup at the Si/SiO<sub>2</sub> Interface in MOS Structures", IEEE Trans. Nucl. Sci., Vol NS-28, No. 6, Dec, 1981
18. R. S. Winokwa and M. M. Solkowski, Appl. Phys. Lett, 28, p 627, (1976)
19. J. F. Wagner and C. W. Wilmsen, "The Deposited Insulator/III-V Semiconductor Interface", Physics and Chemistry of III-V Compound Semiconductor Interfaces, (C. W. Wilmsen ed), Plenum, Ny, 1986 (p 165)
20. A. K. Sinha, H. J. Lewinstein, T. E. Smith, G. Quintana and S. E. Haszko, "Reactive Plasma Deposited SiN Films for MOS LSI Passivation", J. Electrochem. Soc., Vol 125, No. 4, p 601, (1987)
21. E. Doering, "Deposition Technology of Insulating Films" Insulating Films on Semiconductors, ed by M. Schulz and G. Pensl, Springer-Verlog, NY (1981), Proceedings of 2nd International Conference INFOS (81), April 27-29, 1981, Erlanger, Fed. Rep. of Germany, p. 208-218
22. H. J. Stein, IEEE Trans. Elec. Devices, ED-25, 1050 (1978)
23. R. G. Hughes, "Space Charge Effects in Irradiated Si<sub>3</sub>N<sub>4</sub> Films", ECS Symposium Proceedings, Vol 83-8 (ed V. J. Kapoor, H. J. Stein) 1983
24. R. Hezel, "Electron-Beam-Induced-Current Investigations on MOS and MNOS Devices", Solid State Electronics, Vol 22, p 735-742 (1979)
25. R. Hezel, K. Blemenstock and R. Schorner, "Interface States and Fixed Charges in MNOS Structures w/APCVD and Plasma Silicon Nitride", J. Electrochem. Soc., Solid State Science and Technology, July, 1984, Vol 131, No.

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16. Abstract Phosphorus rich plasma enhanced chemical vapor deposition (PECVD) of silicon nitride and silicon dioxide films on n-type indium phosphide (InP) substrates were exposed to electron-beam irradiation in the 5 to 40 keV range for the purpose of characterizing the damage induced in the dielectric. The electron-beam exposure was on the range of $10^{-7}$ to $10^{-3}$ C/cm <sup>2</sup> . The damage to the devices was characterized by capacitance-voltage (C-V) measurements of the metal insulator semiconductor (MIS) capacitors. These results were compared to results obtained for radiation damage of thermal silicon dioxide on silicon (Si) MOS capacitors with similar exposures. The radiation induced damage in the PECVD silicon nitride films on InP was successfully annealed out in an hydrogen/nitrogen (H <sub>2</sub> /N <sub>2</sub> ) ambient at 400 C for 15 min. The PECVD silicon dioxide films on InP had the least radiation damage, while the thermal silicon dioxide films on Si had the most radiation damage.					
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